Design of video acquisition identification system based on Zynq-7000 Soc Platform

Weikang Qian[1,a], Junhui Mei[1,b]

[1]University of Shanghai for Science and Technology, Shanghai Key Lab of Modern Optical System, No.516 Jungong Rd. Shanghai China

[a]elelsec@usst.edu.cn, [b]may.0714@163.com

Keywords: sensor; video acquisition; image processing; FPGA; Zynq-7000

Abstract. This paper Introduced to a practical design method of video acquisition system. It took Zynq-7000 SoC platform's FPGA as the main control chip, OV7670 video sensor as the video source, initialized it by the Serial Camera Control Bus (SCCB) to achieve image acquisition and using edge detection algorithm for image processing of marginalization. Instantiated two asynchronous FIFO module in FPGA chip and combine the SDRAM as data cache to ensure that the VGA display image switching instant, the problem that the changing process of the image data flow may be slow is basically solved. Testing results showed that the system is designed reasonable and be able to satisfy the demand for video data stream output and achieve a better image recognition.

Introduction

Nowadays in the rapid development of embedded system design, there are still a lot of need cannot be met by existing products. Conventional design consists of a single processor, a single ASIC, ASSP, or a simple FPGA program, and the combination of these programs, in some sense, are still unable to meet the requirements for increasingly complex system design. The latest launch of Xilinx Inc, Zynq-7000 Extensible Processing Platform (EPP), integrates dual ARM Cortex-A9 MPCore processor system, programmable logic and hard IP peripherals tightly, providing the perfect combination of flexibility, configurability and best performance. The bright spot of Zynq-7000 EPP is that it contains a complete ARM processing subsystem. That is to say, the processing system is able to boot at boot time (before the FPGA logic) and run various operating systems independent of the programmable logic. So the designers can program on processing system, configuring programmable logic according to the needs. Image acquisition is applied to many high-end products at present and the combination of FPGA and ARM is a common design method. If using Xilinx Zynq - 7000 processing platform, the advantage is that it can be used as FPGA chip and the program expansion in the future is also very convenient.

There are usually two kinds of Image acquisition sensor, CCD sensor and CMOS sensor. They both achieve photoelectric conversion by photosensitive diode, converting images to digital data, and the main difference is the different ways in digital data transfer. Compared with the CCD sensor, as the CMOS sensor has the advantages of small volume, low power consumption, low cost and so on, it is widely used in high-end products. The design discussed In the paper, aim to accomplish the image acquisition and image processing and eventually display video output on VGA, choose the OV7670 of OmniVision company as the CMOS image sensor, Zynq-based FPGA chip as the main control chip, SDRAM as data buffer, and apply the Sobel edge detection algorithm to fringe processing.

System Theory and Design Ideas

The overall system block diagram is shown in Fig.1:

© 2013. The authors - Published by Atlantis Press

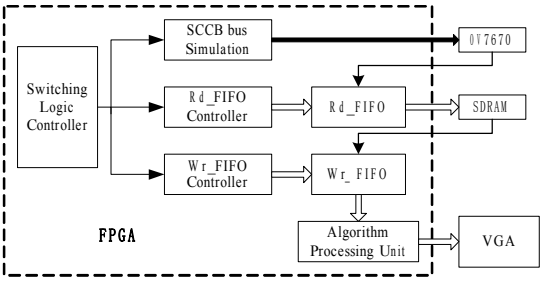

Fig. 1 System Block Diagram

When the system is powered on, FPGA simulates the Sccb bus timing sequence at first to initialize OV7670. The initialization of OV7670 camera includes the configuring of the frame number, the frame pixel and the video export format etc. Then the camera can export video streaming according to the provisions of timing, which flow into FPGA and wait for further processes. At the same time, complete the VGA timing settings according to different screen resolution to fix frame scan time and line scan time, etc. As the camera and VGA are both completed, then it entered into the video data buffer. Since the video data's cross-clock domain transfer, it is needed to be done by FIFO (first in first out) buffer. The buffer module is composed of FIFO, SDRAM, FIFO controller, SDRAM controller and glue logic controller. After the buffering is completed, the video signal output into algorithm processing unit to complete the image processing and the final image will be output to the VGA displayer.

Hardware Logic Design and Verify

Image Sensor OV7670 Initialization**.** The OV7670 is a CMOS image sensor offered by OmniVision company, it provides the full functionality of a single-chip VGA camera and image processor. Support VGA, GIF, and any size scaling down from CIF to 40*30, output support for GRB,RGB,YUV and YCbCr formats, built-in 10-bit dual-channel A/D converter and have automatic exposure control(AEC), automatic gain control (AGC) and other automatic image control functions. The OV7670 provides full-frame, sub-sampled or windowed 8-bit images in a wide range of formats, be controlled through the Serial Camera Control Bus (SCCB) interface. The OV7670 has an image array capable of operating at up to 30 frames per second (fps) in VGA. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control and more, are also programmable through the SCCB interface[1].

Serial camera control bus(SCCB), which has been defined and adopted by OmniVision is a three-wire serial bus structure, to control the functions of vast majority of Series image sensor chip[2]. In simplified pin package, the SCCB bus can be worked in improved two-wire mode with two communication cable ,namely SIO_D (data line) and SIO_C (clock line), SIO_D and SIO_C is equivalent to SCL and SDA of the I^2C protocol respectively[3], The I2C transfer timing is shown in Fig.2.

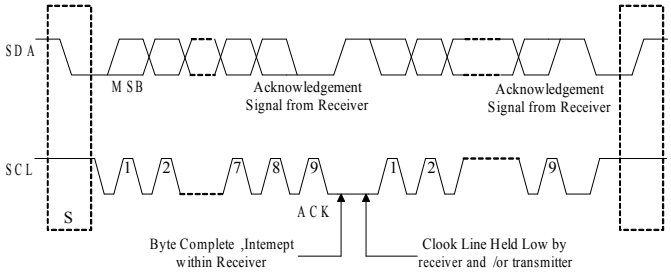

Fig. 2 I^2C transfer timing

The SCCB bus is operation at 10kHz, which is obtained by 100MHz system clock division. The SCCB protocol can be realized by using Verilog HDL programming. The working mode of OV7670 after initialization is 640×480 resolution and 8-bit RGB image data.

Image Buffer Module**.** Because the output frequency of OV7670 is 30Hz, but the SDRAM read and write clock is 100MHz, and the VGA control module clock is 60Hz.In order to synchronize the data transfer between different clock domains, two asynchronous FIFO modules namely Wr_FIFO

and Rd_FIFO is needed to instantiate as data buffers. The main function of the image buffer module is to write the OV7670 output video data to the Wr_FIFO buffer firstly, then written to the SDRAM page by page. Secondly, the video data in the SDRAM buffer is read out to the Rd_ FIFO page by page ,waiting for VGA to get the video refresh data. The FIFO module is realized by Xilinx IP core, its storage width is 16 bit and depth is 64 byte[4]. The buffer module block diagram is shown in Fig.3. In Wr_FIFO, the input ports include wfdata_in, wfdata_in_en and wfdata_in_full, the output ports include wfdata_out and wfdata_out_en, The difference between Rd_FIFO module and Wr_FIFO module is only that wfdata_in_full signal is changed to rfdata_out_empty signal.

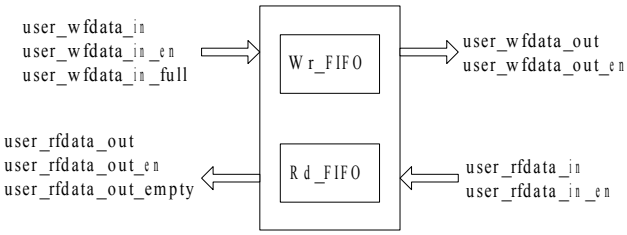

Fig. 3 FIFO module

The output data width of OV7670 is 8bit, in order to take full advantage of the resources and convenient storage of FIFO, 8 bit video data must be converted to 16bit data after through format conversion module processing, 16bit data is written to the Wr_FIFO each operation, written-once 32bytes of data. The input clock of OV7670 is used as the driving clock of Wr_FIFO, the Wr_FIFO enable port is enabled by the row driving signal which is outputted from the camera. In the system, the VGA only use 8bit color as the video output color. Due to the Rd_FIFO module use 16bit data, it needs to adopt a logic converter circuit to convert 16bit data into two 8bit data and output it to the VGA. 32 bytes data is read out to the Rd_FIFO module each operation, and then data will be read out by Rd_FIFO module which is according to VGA timing requirements and displayed on the VGA screen, the write enable port of FIFO is controlled by the written arbitration logic, and read enable port is enabled by the row driving signal of VGA.

SDRAM Memory Control Module**.** The amount of information of the image becomes very large after digitized, so all needs to be stored in external RAM firstly, and then processed by a processor. There are a number of external memory can be used for digital image storage, such as SRAM, DRAM and SDRAM, their capacity and speed of each are different, DRAM and SDRAM belong to the dynamic memory which have great capacity. Because of the CMOS tube is rarely which is used to constitute the storage element in the DRAM, therefore, DRAM chip's capacity is about 16 times of SRAM chip under the same process conditions, so the dynamic RAM is suitable for the large capacity memory because of its high integration, low power consumption and low cost which compares with the static RAM. So the main memory commonly used SDRAM.

The system selected MT46V32M16 as the target memory chips, although MT46V32M16 is DDR1 generation products, the design of the controller have little difference compared with the other two generations products, the basic functions are in place. Controller is divided into four modules from the whole, which respectively is the user interface module, the control module, the data access module and the I/O module.These four module are too vague, and cannot be quickly achieved , so it can continue to be divided, the specific module is shown in Fig.4.

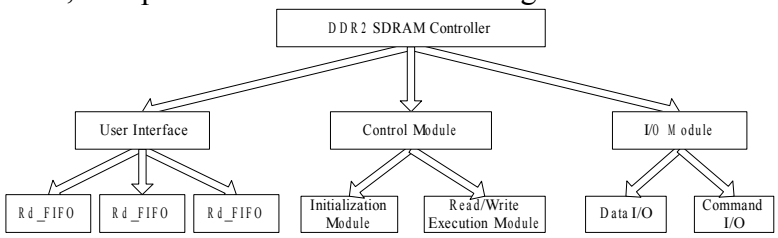

Fig. 4 SDRAM module division block diagram

When the system is powered up or reset, control module will automatically transmit the all initialization commands and the mode loading parameters to the DDR SDRAM after receives the user command, then send read/write commands to the data channel according to the user request which is

used to control the data channel to receive or send data, and send read/write commands to the DDR SDRAM[5]. Data channel mainly completes to send/receive data between user module and DDR SDRAM, read or write is decided by the commands of the controller. The controller response with write/read operation timing are shown in Fig.5/Fig.6. Transfer data and commands between the controller and DDR SDRAM is completed by the I/O module, the control command signal is sent to DDR SDRAM in the same clock edge through the one class register, so it can be sampled by the DDR SDRAM in the same clock edge.

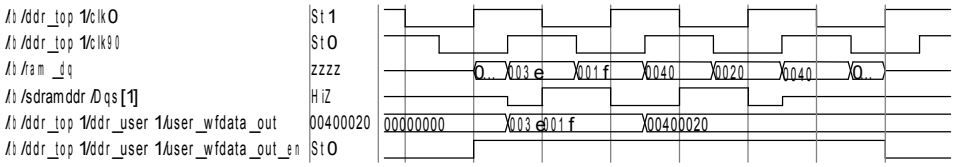

Fig. 5 The controller response write operation timing diagram

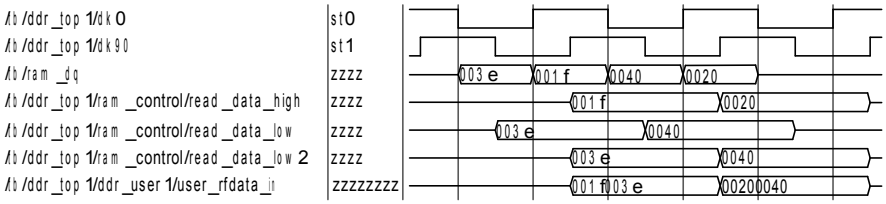

Fig. 6 The controller response read operation timing diagram

The power-on initialization module should be included in the controller because of DDR SDRAM needs to be initialized after each power-up or reset, it can be achieved by a state machine which initialization sequence follows the DDR SDRAM specification. The initialization is divided into two parts, the first part is waiting module, waiting for 200us after power-on or reset, and then release the reset signal, this module will be implemented independently, which will simplify the implementation of the next state machine. The second part is that after the reset signal of first part is released, complete each mode loading and precharge and other commands in sequence[6].

Initial simulation result is shown in Fig.7. The 11 states of the initialization is completed, and generates the corresponding interface signals. the specific mode can be seen in Fig.7.

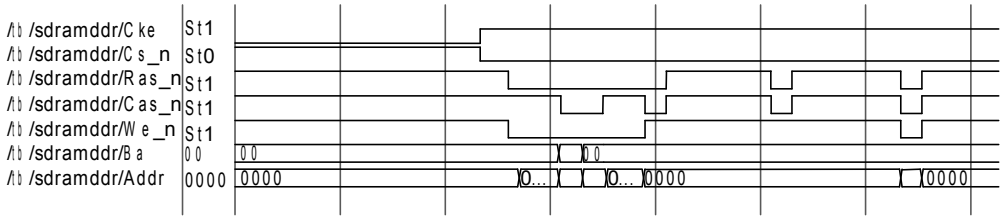

Fig. 7 Initialize simulation diagram

VGA (Video Graphics Array) Display**.** VGA is a kind of Video transmission standard with advantages of high resolution, fast display rate, rich colors, and it has been widely used in the field of color display.

General VGA display unit is consists of three parts, control circuit, display buffer and the video BIOS program. In order to realize the VGA display, it is very necessary to solve the problem of data sources, data storage, and sequential implementation, and the key is how to realize the VGA timing. The system used Verilog HDL to write programs can achieve VGA timing, the VGA resolution is 640×480, and the refresh rate is 60Hz.

The standard reference of VGA display timing is shown in Fig.8. Line timing and field sequential both need to produce four parts, synchronous pulse (a), display back porch (b), active time (c) and display front porch (d).

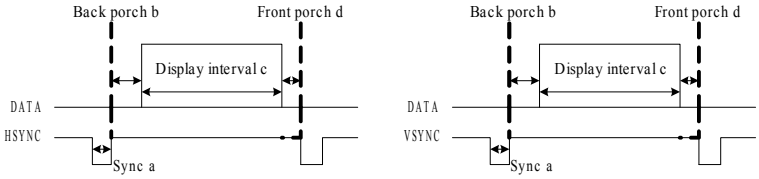

Fig. 8 VGA standard reference sequence diagram

Timing parameters of several common patterns are shown in Table 1

Table 1. Timing parameter table

Image mode	Line timing(us)				Field sequential(lines)			
	a	b	c	d	a	b	c	d
640×480VGA(60Hz)	3.81	1.786	25.635	0.516	63	952	15365	286
640×480VGA(72Hz)	1.28	4.013	20.738.	0.674	80	694	12927	187
800×600VGA(60Hz)	3.22	2.136	20.256	0.930	106	557	16030	---
800×600VGA(72Hz)	2.41	1.223	16.162	1.063	125	438	12596	730

The line synchronous counter Hsync and field synchronous counter Vsync can be realized by using Verilog HDL language, and then it can produce line synchronization and filed synchronization. The code is shown below [7]:

```
always @ (posedge clk or negedge rst_n)
        if(!rst_n) hsync_r <= 1'b1;
        else if(x_cnt == 11'd0) hsync_r <= 1'b0;      // get hsync
        else if(x_cnt == 11'd80) hsync_r <= 1'b1;
always @ (posedge clk or negedge rst_n)
        if(!rst_n) vsync_r <= 1'b1;
        else if(y_cnt == 10'd0) vsync_r <= 1'b0;      // get vsync
        else if(y_cnt == 10'd3) vsync_r <= 1'b1;
assign hsync = hsync_r;
assign vsync = vsync_r;
```

Image Edge Detection Processing

Edge is the most basic features of the image, sometimes objects can be identified only by detecting the edge of the object. The system adopts the Sobel edge detection algorithm to extract the boundary line between the object and background in the image to recognize object. Edge is the results of Pixel brightness values or gray level discontinuity, this discontinuity can be obtained by calculating the gradient of the image, the magnitude and direction of the gradient vector are used to denote the variance rate of gray level and direction.

P_1	P_2	P_3
P_4	P_5	P_6
P_7	P_8	P_9

(a)3×3data window

−1	0	1
−2	0	2
−1	0	1

(b)X- direction

−1	−2	−1
0	0	0
1	2	1

(c)Y-direction

Fig. 9 Sobel operator block diagram

It's the 3×3 area of an image as shown in Fig.9(a), Through the X-direction gradient operator as shown in Fig.9(b) and the Y-direction gradient operator as shown in Fig.9(c) of the Sobel operator to calculate the P5 pixel gradient component which is respectively denoted X-direction gradient and Y-direction gradient[8].

$$G_x = (P_7 + 2P_8 + P_9) - (P_1 + 2P_2 + P_3) \tag{1}$$

$$G_y = (P_3 + 2P_6 + P_9) - (P_1 + 2P_4 + P_7) \tag{2}$$

After calculate the X-direction and Y-direction gradient component, these two components need to be joint together, according to equation (3) to find the absolute magnitude of each point of the gradient.

$$|G| = \sqrt{G_x^2 + G_y^2} \tag{3}$$

In practice, however, according to the formula(4), an approximate magnitude is computed using which is much faster to compute.

$$|G| = |G_x + |G_y| \tag{4}$$

then set up a threshold T, when |G|>T, setting the point of the gray value is 255， on the contrary, the gray value is 0, so that it can be obtained a binarized edge image

Through the above method, it can be seen that the design has good edge detection effect by using modelsim simulation. The simulation result is as shown in Fig.10.

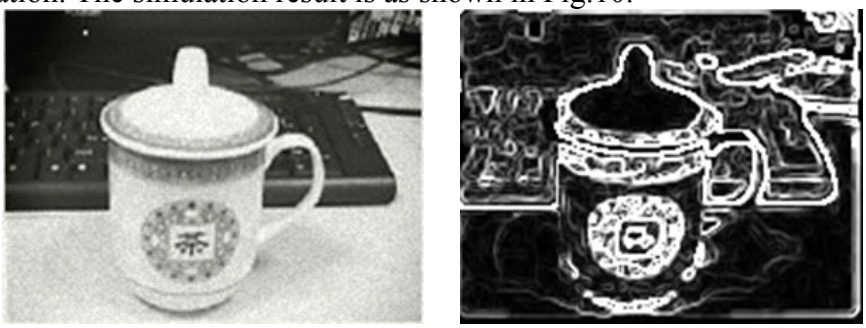

Fig. 10 Original image acquired by system and rendering detected by Sobel edge algorithm

Conclusion

The system design took Zynq-7000 Soc platform's FPGA as the main control chip and initialized video sensor OV7670 by the SCCB bus to achieve image acquisition， because of a large amount of image information, a buffer was needed to receive such a signal. The system used the external SDRAM and combined with the FIFO buffer which was realized by Xilinx IP core as a data cache, then outputted the data to the Sobel algorithm module for processing, and finally displayed on the VGA monitor. The system solved the problem of image is not smooth and realized image recognition function by using the image edge detection processing. This design had great practical value in machine vision research. The tests showed that the system design was reasonable, the hardware structure was simply, it can meet the demand for video data stream output very well and had high practical value.

References

[1] OmniVision Technology. Inc.OV7670/OV7171 CMOS VGA(640×480)CAMERACHIPTM with OmniPixel Technology. Version 1.3.New York;2006.

[2] Song Haizha , Tang Lijun. Xie Xinhui. Image Acquisition and VGA Display Based on OV7620 and FPGA. Video Engineering, 2011(5): 45-47,61.

[3] Lv Tao. Research and design of Digital Image Collection and High-speed Data Transfer Part. Xi'an: Southwest University of Science and Technology, Postgraduate: 2005.

[4] Wu Houhang. Explain the profound theories of FPGA in simple language. Beijing: Beijing University Press, 2010.

[5] Wang Qian, Ding Tiefu. Realization of SDRAM Controller in High-speed Image Storing System. Chinese Journal of Liquid Crystals and Displays, 2006,21(1): 48-52.

[6] Zhou Wangwei, Shi Xiaojun. Design of Double Interface Controller on SDRAM with FPGA. Chinese Journal of Electron Devices, 2006,29(2): 581-584.

[7] Xia Yuwen. Verilog HDL Digital System Design Tutorial. Beijing: Beijing University Press, 2003.

[8] Li Ming, Zhao Xunjie, Mao Weimin. Implementation of Sobel Edge Detection Based on FPGA. Modern Electronics Technique, 2009(16): 44-46.