Noise Optimization of Low Power CMOS Charge Amplifier Using Simulation Environment of Eldo™

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Abstract - A CMOS charge amplifier, due to its very low power consumption and good noise performance, has great interest for analog signal processing in the fields of particle physics, nuclear physics and x- or beta-ray detection. The simulation environment of Eldo™ using AMI05 (American Microsystems Inc.) technology provided by Mentor Graphics Corporation is used for noise optimization of a low power CMOS charge amplifier. Using simulation tools we have designed and simulated the output of the charge amplifier and have calculated the power consumption, band width, gain and Equivalent Noise Charge (ENC) of the circuit. We have also studied the factors on which noise of amplifier depends. This has resulted in a noise performance of ENC = 116 electrons at 0 pF detector capacitance with a power consumption of 80μW per channel. Due to its very low noise and low power consumption, this kind of new charge amplifier can be widely used in research in the fields of Particle Physics, Nuclear Physics and X-ray detection.

Index Terms - CMOS, mentor graphics, Eldo™, low power

1. Introduction

Basically a CMOS charge amplifier is a charge-to-voltage converter, because it converts an input charge signal into output voltage signal. It acts as an amplifier whose equivalent input impedance is a capacitive reactance that is very high at low frequencies. A CMOS charge amplifier does not amplify the electric charge present at its input. Its function is actually to obtain a voltage proportional to that charge and yields low output impedance. Hence it is called a charge to voltage converter.

When a semiconductor detector (a device used to detect or locate the presence of radiations, particles etc.) such as Si used for the measurement of low to high-energy gamma rays and soft X-rays, the output signal is a very weak charge pulse having pulse width of several tens of nanosecond, therefore a preamplifier must be required to amplification of this weak output signal[1].

The total noise contribution of the amplifier is mainly determined by the input transistor[2]. The input transistor is the main device which tunes the noise; the contributions of the other transistors cannot be completely neglected though. The dimension of these transistors has therefore been optimized with respect to their noise behavior[3]. The choice of the input transistor as well as its bias current is very important. Normally the noise performance of the input transistor is mainly characterized by an equivalent input noise voltage source V_e with noise spectral density (equivalent input noise voltage source)[2].

Hu et al.[4] reported the (ENC) noise performance of 343 electrons at 0pF with a noise slope of 28 electrons/pF for a peaking time of 10μs. A 37mV/fC conversion gain, 3.5V power supply and 150μW/channel power consumption was obtained. Nygard et al. [5] reported ENC of 112 electrons at 0pF with a slope of 34 electrons/pF for a power consumption of 1mW. Hu et al. [6] reported theoretical results that show a total output noise voltage reduction of 0.264mV. A measured noise performance of 450 electrons at 0pF with a slope of 45ns, a conversion gain of 20mV/fC and 1mW power consumption was obtained. Berst et al.[7] presented a noise performance of ENC=330e^-+51e^-/pF for a peaking time of 100ns. The simulations were performed for the devices to be used in future LHC experiments, and an ENC noise slope of 37 electrons/pF has been obtained, with power consumption of 1mW per channel for shaping time of 25ns[8].

We have designed a schematic of CMOS Charge Amplifier and have run on Eldo™ Simulator and then checked its behavior on EZ-waves by using IC Nanometer Design software (designed by Mentor Graphics Corporation). The following three important key points were kept in mind that can improve the low noise, tranconductance, speed of amplifier and flicker noise.

- The dimensions of input transistor act as a key by which we control the noise of charge-amplifier.
- The FET on the output must be small in order to realize high speed of charge amplifier.
- In order to minimize the intrinsic noise, a PMOS transistor has been chosen as input transistor due to its lower flicker noise compared to the corresponding NMOS transistor.

2. Results and Discussion

Most important parameters and constants that have been selected for these simulations are summarized in Table.1.

By using the design architect graphics and tools and by following the important points explained above, we created a schematic capture of CMOS charge amplifier circuit as shown in Figure 1. By using AMI05 technology, Transient Analysis result obtained is shown in Figure 2.

Table.1. Charge Amplifier Design Parameters and Constants

Symbol	Description	Selected Values
W/L	Input transistor (T_1) dimension	1000µm/0.25µm
C_f	Feedback capacitance	0.6pF
C_i	Input capacitance	78.73pF
C_d	Detector capacitance	0pF
V_{DD} & V_{SS}	Power supply	V_{DD}=+2V, V_{SS}=-2V
I_d	Bias current	20µA
K_f	Flicker noise coefficient	$5x10^{-9}fC^2/\mu m^2$
C_{ox}	Oxide capacitance	$6.4fF/\mu m^2$
K	Stefan-Boltzmann constant	$1.38x10^{-23}J.K^{-1}$
T	Absolute temperature	300K
K_P	Transconductance constant	$6.42x10^{-7}A/V^2$
Q_{in}	Input current pulse	22000e^- or 3.52fC
g_m	Transconductance constant	0.315mA/V
R_f	Feedback resistance	~48MΩ

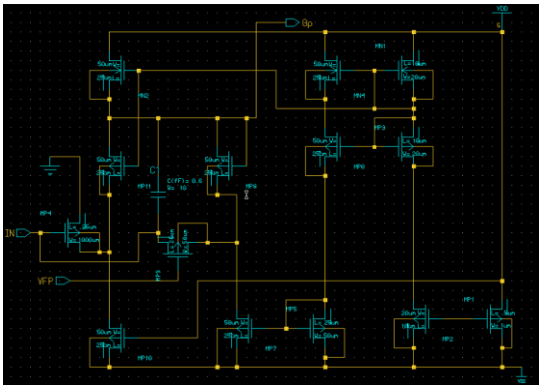

Fig.1. Schematic of CMOS Charge Amplifier Circuit

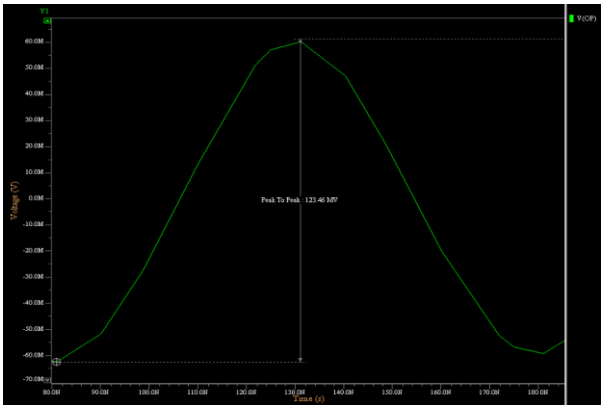

Fig.2. Transient Analysis result, using AMI05 Technology

Our designed charge amplifier circuit is an analog amplifier circuit as can be seen from the shape of the curve in this figure. From Figure 2, we obtain peak-to-peak voltage of Vout=123mV. Vout calculated here along with Table.1 can be used to arrive at:

A_{qv} = 34.94 mV/fC

Now we also find the voltage gain (A_v) of charge amplifier that comes out to be A_v = 0.2469. As $V_{in} > V_{out}$ and $A_v < 1$ (i.e. output voltage of signal reduced from input voltage of signal, so it is a power amplifier which increase the power of weak input signal.

By using AMI05 technology, AC-Analysis result is obtained as shown in Figure 3. Our designed circuit behaves like a low-pass filter circuit. Cutoff frequency (W_c) is the frequency at which voltage gain is equal A_v = 0.707 of maximum value.

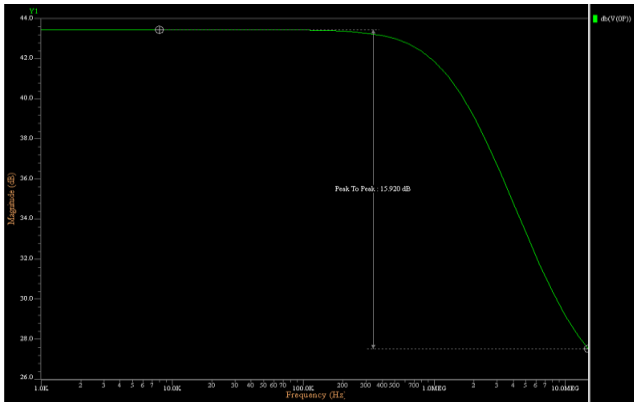

Fig. 3 . AC - Analysis result, using ami05 Technology

From Fig. 3:
Cutoff frequency (W_c) = 900 kHz
Lower cutoff frequency (f_1) = 1 kHz
Upper cutoff frequency (f_2) = 900 kHz
Band width (BW) = 899 kHz

We calculated the values of spectral density (Svn) corresponding to different frequency values and plotted these, as shown in Figure 4.

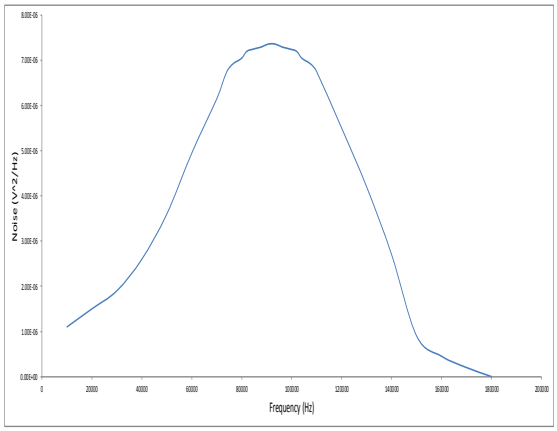

Fig. 4. Output noise spectral density

As the optimized noise performance is present in Figure 4 from which we obtained system noise band width Δf= 63 kHz by which the total rms output noise voltage V_n total is calculated.

From the values in Table 1 and using various standard equations, we get the resultant values for our designed charge amplifier. These values are summarized in Table 2 below.

Table.2. Eldo™ simulation results summary for a CMOS charge Amplifier (using ami05 technology)

Power supply	VDD = +2V, VSS = -2V
Bias current (Ids)	20 μA
Power consumption (p)	80 μW
Tranconductance (gm)	0.315 mA/V
Conversion gain (Aqv)	34.94 mV/fC
Equivalent Noise Charge (ENC)	116 e- at Cd = 0 pF
Voltage gain (Av)	0.247
Cutoff frequency (Wc)	900 kHz
Band width (BW)	899 kHz
Input current pulse (Qin)	22000 e- or 3.52 fC

3. Conclusions

In this work, noise optimization of low power CMOS charge amplifier using simulation environment of Eldo™ has been presented. Simulation results show that a noise performance (ENC) of this charge amplifier is ENC = 116 electrons at 0 pF detector capacitance has been obtained with a power consumption of 80μW per channel. Due to its very low noise and low power consumption, this kind of charge amplifier can be widely used in particle physics, nuclear physics and x-ray detection.

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