VHDL Implementation of a prototype switching system

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Abstract

Switching system implies data transmission between two communicating entities. This transmission can be either via trunks or it can be completely wireless, technically termed as Telephone Switching and Mobile switching, respectively. We report the implementation of a switching system using very high speed integrated circuit hardware description language (VHDL) which is more reliable and efficient than the present switching system. It converts entire bulky switching unit which consists of routers, multiplexers, decoders, counters in to a single integrated circuit (IC). Simulation results are presented for transfer of data from input subscriber to the output subscriber using sequential write /random read mode with the timing diagram. To verify the transfer of data from input subscriber to the output subscriber a 16 bit op-code is assumed in which each bit represents a specific function.

***Keywords*: — Switching system, VHDL, Control memory, Data memory and Op-code**

1. Introduction

In present scenario of the technology, there are two fields in engineering that hold great demand in the industry; communication and VLSI. The people want to connect themselves to anyone, anytime and anywhere. We have already experienced a huge development from a simple morse code telegram to the highly sophisticated triple play broadband ISDN, or nonetheless the Satellite Communication. This might give you ways to communicate with speech, that's no big deal; in fact the amazing part starts when real time audio, video and data can be integrated for communication. But at present there is also a second stringent demand that is miniaturization. The race is on for reaching the minimum space as much as possibly occupied by the systems. This paper, keeping an eye wide open on the future, has mixed both fields enabling us to communicate, in a digital manner, by using systems that

would be integrated on an IC through programming of the IC using VHDL.

VHDL is a language for describing digital electronic systems. There was a need for a standard language for describing the structure and function of integrated circuits (ICs). Hence the VHDL was developed, and subsequently adopted as a standard by the Institute of Electrical and Electronic Engineers (IEEE) in the US. VHDL is designed to fill a number of needs in the design process. Firstly, it allows description of the structure of a design that is how it is decomposed into sub-designs, and how those sub-designs are interconnected. Secondly, it allows the specification of the function of designs using familiar programming language forms. Thirdly, as a result, it allows a design to be simulated before being manufactured, so that designers can quickly compare alternatives and test for correctness without the delay and expense of hardware prototyping [1].

This paper focuses more on the programming part rather than the hardware. We have explained every model in detail with their opcodes (user defined), underlying architecture and programming. Along with that the simulation results are also provided, showing transfer of data from input subscriber to output subscriber using sequential write/ random read method with timing information. To verify the transfer of data from input subscriber to the output subscriber a 16 bit op-code is assumed in which each bit represents a specific function.

II. WORKING SPECIFICATIONS

A. Features

- Dual way 16 user support
- Sequential Input Random Read
- Caller Id Facility
- Inter and Intra exchange
- 8 Bit data transfer
- In band Signaling
- Synchronization clock
- Reset features.

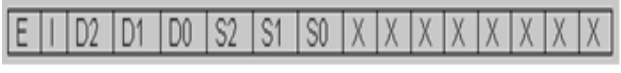

Fig. 1 16 bit opcode

The opcode assumed is of 16 bit in which each bit is having some specific function. Starting from right hand side, the bit 0 to 7 represents data, bit 8-10 represent source subscriber, bit 11-13 represent destination subscriber, bit 14 represent whether the call is interexchange or interexchange and bit 15 represent whether the subscriber is enabled or disabled.

B. Principle of Landline Switching

In this design, the data coming in through the inlets are written into the data memory and later read out to the appropriate outlets. The incoming and out coming data is usually in serial form whereas the data are written into and read out of the memory in parallel form. It therefore becomes necessary to perform serial to parallel conversion and parallel to serial conversion at the inlets and outlets respectively. For convenience, the in and data out parts of the MDR are shown separately for the data memory. Since there is only one MDR a gating mechanism is necessary to connect the required inlet/outlet to MDR. This is done by the in gate and out gate units. The information is not transferred in real time: it is first stored in the memory and later transferred to the outlet. [8].

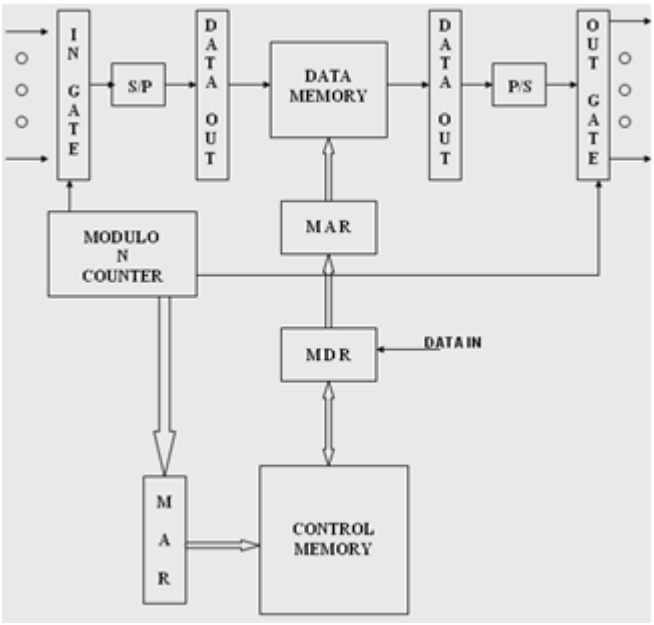

Fig. 2 Structure of the Switching System

This switching system can be controlled in following three ways:

- Sequential write/Random read.
- Random write/Sequential read.
- Random input/Random output.

In the first two methods of control, the sequential / random read / write operations refer to the read / write operations associated with the data memory. In both these cases, the inlets and outlets are scanned sequentially. In the last case, the inlets and outlets are scanned randomly, and the data memory is accessed sequentially. There are two modes in which this switching system may be operated under any of the three forms of control. We term these modes as:

- Phased operation
- Slotted operation

But we are concerned only with the phased mode of operation.

C. Results and Discussion

The simulation results for the switching structure are shown in Fig. 3 and Fig. 4, which verified the successful data transfer from input subscriber to output subscriber using sequential write/ random read method in phased mode. The Model-Sim simulator is used for the verification of results [2].

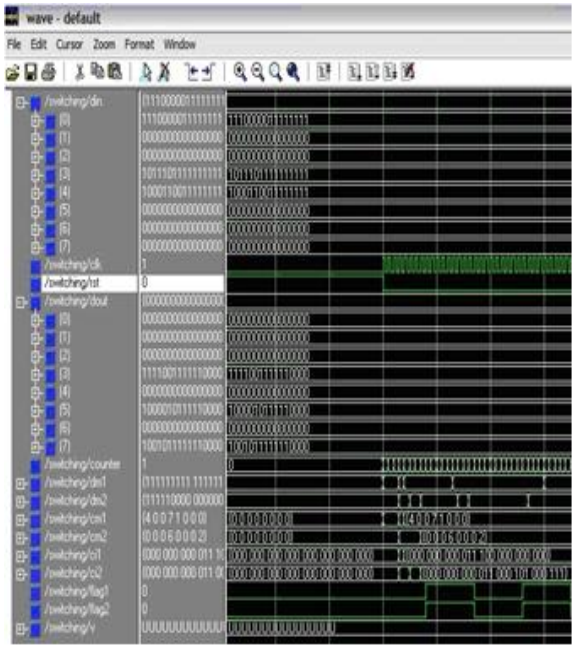

Fig. 3 Phase 1 (Sequential Write)

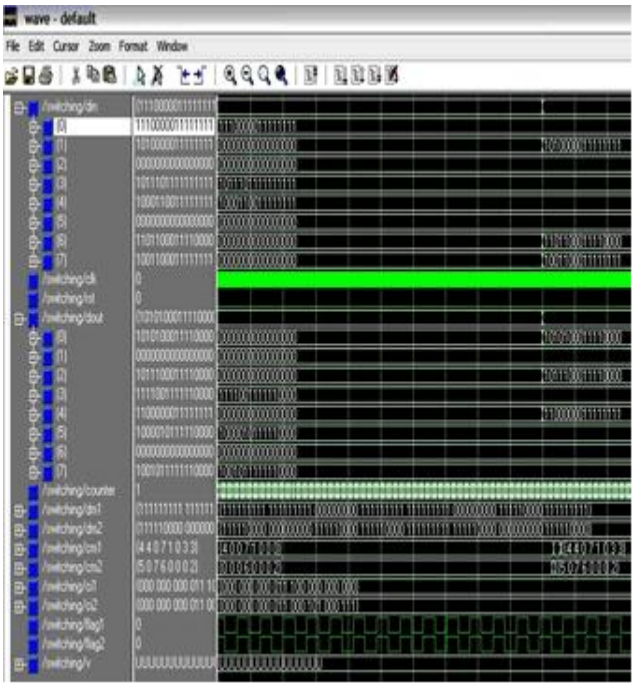

Fig. 4 Phase 2 (Random Read)

D. Phase 1

Input Subscribers in both the exchanges are scanned sequentially. It takes 8 clock cycles to scan 16 subscribers in order to know their status, i.e. they want to transmit or not. This is called a sequential scanning. The data to be transmitted is stored in data memory (8x9) in sequential order. The information relating to the called subscriber is stored in control memory (8 locations of integer type) in sequential order and caller id number is stored in the caller id memory (8x3) in the same way. Thus, system is sequential write.

E. Phase 2

When all the scanning is finished, the location of the data memory is read according to the corresponding location of the control memory. For example, if first location of data memory has data ‘d’ and corresponding location in control memory is 2, this means that ‘d’ will be communicated to the 2nd user of the exchange, thus, the system is random read.

To decide where the data will be communicated, we use a bit in our opcode as ‘I’ bit. If ‘I’ =1, then it is interexchange, i.e. the read out data, will be given to user of other exchange. Thus communication between the subscriber of two exchanges can be made possible and hence the name interexchange. If ‘I’ = 0,

then it is called as intraexchange, i.e. the read out data, will be given to the user of the same exchange. Thus communication between subscribers of the same exchange is made possible, and hence the name Intraexchange.

The exchange between caller id memories is done only, if the particular user is enabled. Same is the case with data memory. A particular user is enabled, if its opcode 16th bit is 1 and disabled if it is 0. So caller must be enabled and called must be disabled in order to make a call successful. The communication means just to transfer the data (0- 7 bits of opcode) between entities and is shown by overwriting the data bits if called sub=scriber. Caller id facility enables the called user to see who is calling by checking his relevant bits of opcode (13 to 11).

III. CONCLUSIONS

VHDL has been used to write all the programs for the IC's because of its user-friendly nature and thus modifications if required for further development shall not prove to be an obstacle. As we know, the process of making IC's is time consuming and an expensive venture, so we must be sure about the working results of the IC's in advance as we can't accept errors later. Thus the paper focuses on simulation prior to fabrication. This paper is a significant effort towards total digitization of switching exchanges and would surely prove a boon for VLSI design industry.

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