

Wireless Feature Extraction System for Cloud-Dust Based Intelligent System by Using Embedded Wavelet Packet Method

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Abstract

In the paper, a wireless feature extraction system for cloud-dust based intelligent system using embedded wavelet packet method is developed. In order to decrease the massive transmission data form receivers and transmitters of wireless sensors network, we reduce the data dimensions of sensors using embedded feature extraction method. The massive transmission data will be reduced via the process of wavelet packet decomposition and reconstruction. So it decreases the transmission loading of general wireless sensors network. Considering computing time of feature extraction, the circuit hardware of wavelet packet is designed in the paper. It effectively reduces the computing time of feature extraction. Therefore, the wireless feature extraction system using embedded wavelet packet method makes the transmission of wireless sensors network work effectively. At last, we prove the data reduction of transmission, the shorter computing time of feature extraction and the computing accuracy of wavelet packet hardware by the experiments. It can greatly improve wireless sensors network with large number of nodes more efficient transmission, and the sampling rate of sensors nodes, without causing the

transmission delay and data errors. So it will make wireless sensors network more applications with higher precision, higher computing speed, lower power and lower cost in the future.

Keywords: Feature Extraction, Wavelet Packet, Wireless Sensors Network, Verilog-HDL

1. Introduction

For cloud-dust based intelligent system, a wireless feature extraction (FE) system (WFES) using embedded wavelet packet (WP) method is developed in the paper. A cloud-dust based intelligent system is an intelligent system using cloud computing combined many embedded systems. In general, the transmission performance is the important specification of the wireless sensors network (WSN). In order to decrease the massive transmission data form receivers and transmitters of WSN, we reduce the data dimensions of sensors using embedded FE method. In 2011, Y.L. Borgne [1] proposed a Unsupervised and supervised compression with principal component analysis in WSN, allowing to extract a maximum of variance while keeping the network load bounded, and to reduce the network load while keeping

the approximation error bounded Present two operating modes, unsupervised and supervised, and the efficiency of the proposed approach in a realistic WSN deployment for temperature monitoring. In 2010, C.C. Huang [2] develops hardware architecture of FE using WP method for an intelligent diagnostic system. Verilog-based FE architecture is proposed and implemented. The test results of samples of different rotating speeds under the normal and eccentric spindle states show the effect of the hardware of FE and verify the feasibility of hardware design. In 2002, S. Madden [3] proposed a Tag: a tiny aggregation service for ad-hoc sensors networks. In fact, data aggregation techniques are used for reducing the number of data transmissions by distributing the function which needs all sensors' observations throughout the network, so each node shall apply the function to its received values. Summarize the above development, in this study, the WSN combination of FE using WP method can effectively reduce data dimensionality of sensors network.

2. Wireless Feature Extraction System

2.1. System Architecture

In this study, the hardware architecture of FE system using WP method can rapidly compute and transmit data in the WSN (ZigBee). For decreasing the massive transmission data form receivers and transmitters of WSN, we reduce the data dimensions of sensors using FE method. The architecture of WFES is shown as figure 1. The FPGA-Based development board is used to fetch data from sensors of motors, robots, and CNCs. And then it computes the value of the features for decreasing the transmission data size.

2.2. System Flowchart

The flowchart of WFES is shown as figure 2. The transmitter and receiver of the WSN (ZigBee) transmit and receive data of sensors nodes each other. The sensors are usually installed on motors, robots, CNCs... etc. Before transmitting, data of sensors is processed using the decomposition and reconstruction of FPGA-Based WP each node.

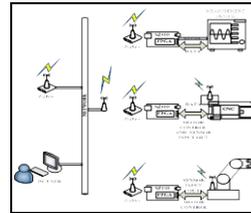


Fig. 1: Architecture of WSN (Zigbee).

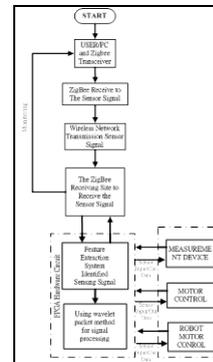


Fig. 2: The flowchart of the WFES.

3. Wavelet Packet Method

3.1 Wavelet Packet

The massive transmission data will be reduced via the process of WP decomposition and reconstruction. So it decreases the transmission loading of general WSN. In this study, Daubechies WP [4] is used for the decomposition and reconstruction of the high frequency signal and low frequency signal. Daubechies wavelet is a continuous orthogonal wavelet which is solved into the scale formulas and wavelet function with the scaling coefficients and wavelet

coefficients by multi-resolution analysis formula [5]. The process of WP decomposition is shown as figure 3.

3.2 Feature Extraction

There are many methods for the dimensions reduction of massive data, such as Principal component analysis (PCA), Linear Discriminant Analysis (LDA), Karhunen-Loeve Transform (KLT)... etc. And these several methods can be used for FE. In this study, we chose the WP method for FE. The main reason for the selection is that WP can decompose and reconstruct a large number of signal data into the high and low frequency signal for the amount of data dimensionality reduction. The architecture and flowchart of FE using WP is shown as figure 4 and figure 5. The massive data will be reduced by the decomposition and reconstruction of WP so that the transmission loading is decreased in the WSN.

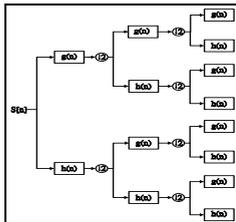


Fig. 3: Wavelet packet signal decomposition.

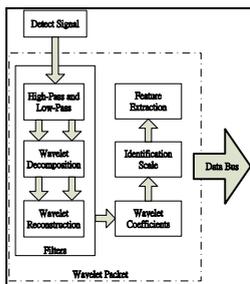


Fig. 4: Architecture of feature extraction.

4. Hardware Design

Considering computing time of FE, the circuit hardware of WP is designed in the paper. In this study, we use behavior design for hardware circuits of FE system using WP in Verilog-HDL. It can make the complex circuit to interpret and modify easily. The design concept is based on bottom-to-top design approach consists of several basic modules. The hardware circuit modules of FE system using WP is a large module designed from a combination of many small modules, so that the entire modular architecture can reduce the design work. The architecture of hardware circuit makes the computing of WP faster and faster. The hardware circuit architecture of WP is shown as Figure 6.

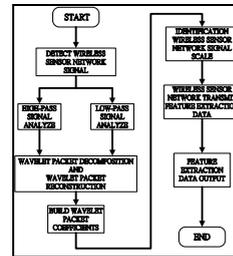


Fig. 5: Flowchart of feature extraction

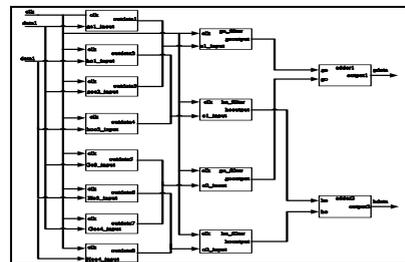


Fig. 6: Hardware architecture module of WP.

5. Results and Discussions

In the study, the WSN combined FE is proposed. We compared the results of the experiments between the executions of software (Matlab) from WP hardware circuit (ModelSim). The simulation of FE showed the data reduction, computing speed and computing accuracy.

5.1 Comparison of Testing Results

5.1.1 Data Size for Transmission

In this section, we will do the comparison of data size before and after using WP method. As figure 7 shown, the original transmission data is larger than the reduced data using WP method. The original transmission data are near 250k and the reduced data using FE method are about 150k. It means that the data transmission will be more efficient after reducing data size by FE.

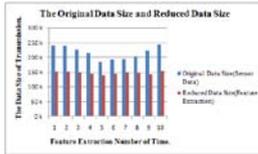


Fig. 7: The original and FE data size.

5.1.2 Computing Speed of FE

This experiment is test for the computing speed of FE system in the software and hardware environment. After the test, the computing speed of the hardware-based FE system is much faster than the speed of the software-based FE system. It is shown as Table 1.

Tab. 1 Comparison of Computing speeds

FE No.	A	B	C	D%
1	0.512ms	0.420ms	0.080ms	15.62%
2	0.554ms	0.442ms	0.112ms	23.49%
3	0.477ms	0.427ms	0.095ms	10.40%
4	0.434ms	0.380ms	0.048ms	9.21%
5	0.768ms	0.640ms	0.120ms	15.62%

A: WP Value by MATLAB FE Computed, B: WP Value by Circuit FE Computed, C: Error, D: Accuracy Error

5.1.3 Computing Accuracy of FE

This experiment is test for the computing accuracy of FE system in the software and hardware environment. The computing accuracy of the hardware-based FE system and the software-based FE system is shown as Table 2.

Tab. 2 Accuracy of feature extraction

FE No.	FE (Software Computing Speed)	FE (Hardware Computing Speed)	Faster Rate(%)
1	0.254 us	0.217 ms	117k %
2	0.342 us	0.311 ms	109k %
3	0.354 us	0.284 ms	124.6k %
4	0.251 us	0.117 ms	214.5k %
5	0.242 us	0.129 ms	187.5k %

6. Conclusions

By the experiments, it showed the advantages of the system are the data reduction of transmission, the shorter computing time of FE and the computing accuracy of WP hardware. It can greatly improve WSN with large number of nodes more efficient transmission, and the sampling rate of sensors nodes, without causing the transmission delay and data errors. So it will make WSN more applications with higher precision, higher computing speed, higher reliability, lower power and lower cost in the future. Therefore, the WFES using embedded WP method makes the transmission of WSN work effectively.

7. References

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