

Design of Unsymmetrical Doherty Power Amplifier for 460MHz LTE-Advanced Applications

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Abstract—An unsymmetrical Doherty power amplifier (DPA) at 460MHz is presented in this paper. The carrier and peaking amplifier of the DPA, which base on two equal-sized devices, are matched with different networks to mitigate the performance degradation caused by the limited load modulation. Measured with continuous wave (CW), the unsymmetrical DPA saturates at an output power of 49.2dBm and achieves a drain efficiency of 51% at 6dB back-off. Using a one-carrier long term evolution advanced (LTE-Advanced) signal with 20MHz bandwidth, the unsymmetrical DPA exhibits a drain efficiency of 48.7% at an average output power of 42.1dBm, along with adjacent channel leakage ratio (ACLR) of -34.1dBc and -53.3dBc before and after digital pre-distortion (DPD), respectively.

Keywords- unsymmetrical; Doherty power amplifier; output matching networks; LTE-Advanced

I. INTRODUCTION

Modern communication systems employ complex modulation schemes to increase the data throughput and enhance the network capacity. Unfortunately, envelopes of the modulated signals in such systems may vary widely and rapidly, and resulting in high peak to average power ratio (PAPR) [1]. The power amplifier is forced to operate far from its saturation region to satisfy the linearity requirements for the systems, at the cost of drastically decrease in the power efficiency. Therefore, power amplification architecture with significant efficiency enhancement at back-off operation is essential and urgent [2].

Several architectures have been proposed to improve the power amplifier efficiency at power back-off region[3]. Compared with other approaches, the Doherty technique, with advantages such as high back-off efficiency, low circuit complexity, and proven linearizability, draws a lot attention and has been widely investigated. The convention DPA consists of two amplifiers: the class AB biased carrier amplifier and the class C biased peaking amplifier. It exploits the inbuilt active load modulation as a function of the input signal level to maintain constant efficiency in the power back-off range. Due to lower bias voltage, the peaking amplifier contributes less output power than the carrier amplifier in the convention topology, the load impedances cannot be fully modulated , eventually cause performance degradation [5].

In this paper, we design and implement an unsymmetrical DPA using two equal-sized devices for LTE-A systems. Unsymmetrical architecture is adopted to improve the load modulation. Analysis and design of unsymmetrical DPA is given in section II, followed by implement and experimental results of the proposed DPA. A conclusion is given in Section IV.

II. ANALYSIS AND DESIGN OF THE PROPOSED DPA

To overcome the issues related to limited load modulation in the conventional DPAs, unsymmetrical architecture is utilized, which is implemented by using two equal-sized devices with unequal saturation power resulting from different output matching networks. In this section, the operational principle of the unsymmetrical DPA is analyzed, followed by detailed design procedures of the proposed DPA.

A. Analysis of the Proposed DPA

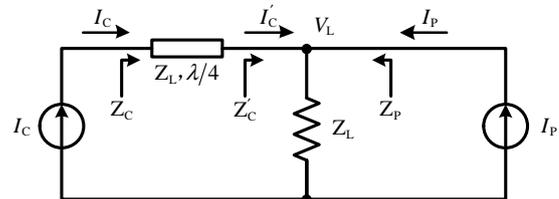


Figure 1. Operational diagram of the Doherty amplifier

Figure 1 shows the equivalent circuit diagram commonly used to analyze the operation of Doherty amplifier. Current I_C' reaches maximum value and remains unchanged in the medium power region due to the characteristic of $\lambda/4$ transformer [8], where $I_C(\theta_C)$ denotes the maximum fundamental component of drain current of carrier amplifier at peak power region. Thus, the fundamental current of carrier amplifier and peaking amplifier at joint point P can be written as[9]

$$I_C' = \frac{I_{C,\max}}{2\pi} * \frac{\theta_C - \sin \theta_C}{1 - \cos(\theta_C/2)}, V_{in,\max}/2 \leq v_{in} \leq V_{in,\max} \quad (1)$$

$$I_P = \frac{I_{P,\max}}{2\pi} * \frac{\theta_P - \sin \theta_P}{1 - \cos(\theta_P/2)}, V_{in,\max}/2 \leq v_{in} \leq V_{in,\max} \quad (2)$$

where θ_c and θ_p are the conduction angles of the carrier and the peaking amplifier respectively, and are related to the bias condition and input power level[8].

As defined in[8], the back off power (B.O.P) can be written as

$$\text{B.O.P} = -20 \log(\alpha) = -20 \log\left(\frac{I'_c}{I'_c + I_p}\right) \quad (3)$$

let ξ denotes the ratio of I_p to I'_c , by using (1), (2) and (3), ξ can be rearranged as

$$\xi = \left(10^{\frac{\text{B.O.P}}{20}} - 1\right) = \frac{I_{p,\max}}{I_{c,\max}} * \frac{\left(1 - \cos \frac{\theta_c}{2}\right) * (\theta_p - \sin \theta_p)}{\left(1 - \cos \frac{\theta_p}{2}\right) * (\theta_c - \sin \theta_c)} \quad (4)$$

According Eqn. (4), B.O.P is related to $I_{c,\max}$, $I_{p,\max}$, θ_c and θ_p . Therefore, for a specified B.O.P, load modulation can be improved by minimizing the difference between θ_c and θ_p with gate bias adaption or uneven power split, or by using two unequal-sized devices, the one with larger I_{\max} used in the peaking amplifier. Furthermore, this could also be achieved by optimizing the output matching networks of the carrier and peaking amplifier, especially when equal-sized devices are used. With the optimized output matching networks, the peaking amplifier was matched to the impedance of maximum output power, while the carrier amplifier was matched to the impedance of maximum efficiency in back-off region.

B. Design Procedures of the Proposed DPA

Design procedures of the unsymmetrical DPA based on identical device are as follows.

Step1 Specifying the B.O.P;

Step2 Determine the optimum load impedance $Z_{\text{peaking, opt}}$ for the peaking amplifier to generate maximum output power $P_{\text{peaking, max}}$;

Step3 Calculate the maximum output power of the carrier amplifier $P_{\text{carrier, max}}$ according Eqn. (3);

Step4 Determine the optimum load impedance $Z_{\text{carrier, opt}}$ and $2 * Z_{\text{carrier, opt}}$ for the carrier amplifier to deliver output power $P_{\text{carrier, max}}$ and achieve maximum efficiency in back-off region respectively;

Step5 Design the matching networks and fine tuning the gate bias voltages of the carrier and peaking amplifier.

Tuning of the gate bias voltages for tradeoff between linearity and efficiency and easiness to matching networks design should be taken into account when selecting the optimum load impedances. And impedances locate on the line where the constant power contours are sparsely distributed are much more preferred in case of impact of the temperature variation on the performance of the DPA.

III. IMPLEMENTATION AND EXPERIMENTAL RESULTS

A. Implementation

As shown in Figure 2, The unsymmetrical DPA was fabricated on a 30mil thick Rogers RO4350B substrate with a 3.48 dielectric constant. The carrier and peaking amplifier are realized using LDMOS devices MRFE6S9045N from Freescale. The gate bias voltages of the carrier and peaking amplifier are tuned to make a tradeoff between efficiency and linearity. And the bias for the carrier amplifier is $V_{ds_C} = 28V$, $V_{gs_C} = 3.10V$, while $V_{ds_P} = 28V$, $V_{gs_P} = 2.05V$ for the peaking amplifier.

Followed the design procedure as described earlier, the optimum impedances, $Z_{\text{peaking, opt}}$, $Z_{\text{carrier, opt}}$ and $2 * Z_{\text{carrier, opt}}$ are determined from a load pull simulation to be $(3.45 + j4.57)\Omega$, $(4.82 + j2.54)\Omega$ and $(6.27 + j5.63)\Omega$, respectively. Bias the peaking amplifier and the carrier amplifier at the same voltage, $V_{ds} = 28V$, $V_{gs} = 3.10V$ ($I_{ds} = 460 \text{ mA}$), saturation power of 47.2dBm and 46.3dBm are obtained respectively.

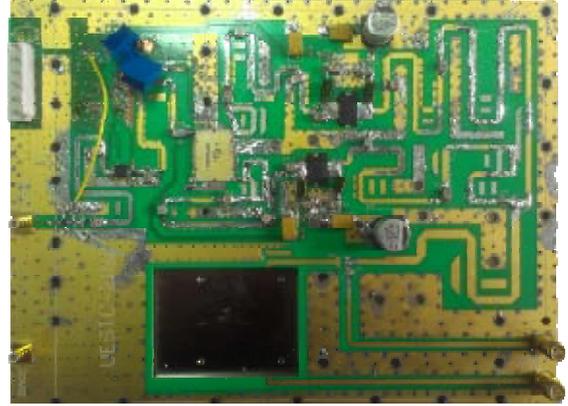


Figure 2. A photograph of the manufactured wideband Doherty amplifier

An 22pF capacitor and a 8.2Ohm resistor were parallel inserted into input matching network to stabilize the amplifier, and an additional 6.2Ohm resistor was placed in the gate bias networks to make the DPA more stable, at the cost of decreased overall gain. A 22nH inductor was inserted between the power supply and gate or drain ports as RF chock, taking the place of $\lambda/4$ inverter to reduce the size of the DPA circuits. Four 47pF capacitors was shunt to the ground between the 22nH inductors and power supply to serve as decoupling capacitors. And the bias networks were partially absorbed in the matching networks for better performance and lower cost.

To minimize the phase difference between the carrier amplifier and the peaking amplifier, the topology of the output matching networks for both cells are identical. For different matching purpose, the value of the shunt and serial capacitors in the matching network differs. The PCB and the devices such as transistors and power splitter are solder on the heat sink for better thermal conductivity and reduction of memory effects.

B. Experimental Results

Measured with CW signal at 460MHz, the proposed DPA shows an saturation output power 49.2dBm (83.2W) and peak drain efficiency of 70.6% and 6dB back-off drain efficiency of 51%. Pre-driven and driven by HMC589 and MMG3006NT1, the gain of the lineup amplifier is about 58dB. And as the input power increase, the gain of the DPA gradually increase, which result from higher bias voltage of the peaking amplifier, and inevitably cause the decrease of the drain efficiency.

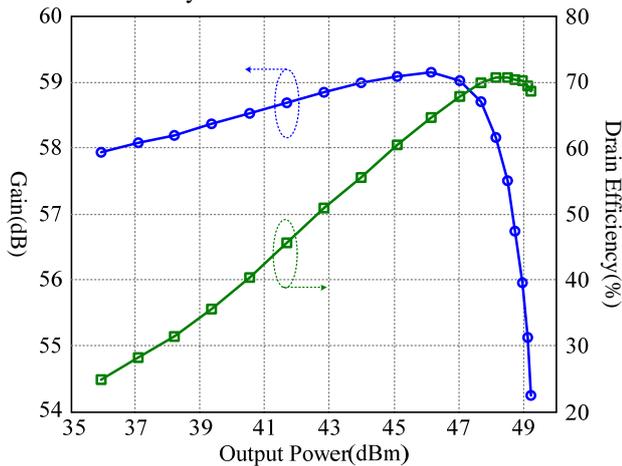
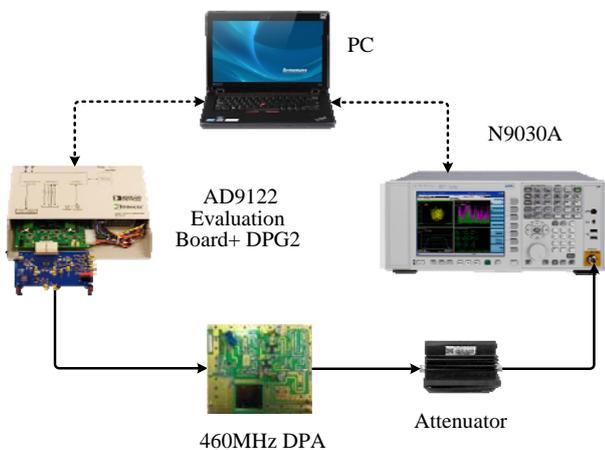


Figure 3. Measured gain and drain efficiency of the proposed DPA with 460MHz CW signal



Setup of the DPD correction system

To characterize the linearity of the proposed Doherty power amplifier LTE-A signals, the digital pre-distortion correction system shown in figure 4 is employed. One carriers 64-QAM modulated LTE-A signals with totally 20MHz bandwidth are generated in the personal computer (PC) and the PAPR is reduced to 6.8dB after crest factor reduction (CFR). The I/Q baseband signals are downloaded into the AD9122 evaluation board and upconverted to RF signals. The RF signals are amplified by preamplifier and wideband DPA, and then downconverted and demodulated by Agilent signal analyzer N9030A after attenuation. Inverse PA modeling is carried out in the PC with the I/Q data

acquired in the N9030A. With the inverse PA mode, the pre-distorted signal can be generated and then downloaded into the AD9122 evaluation board again as the input signal for DPD correction.

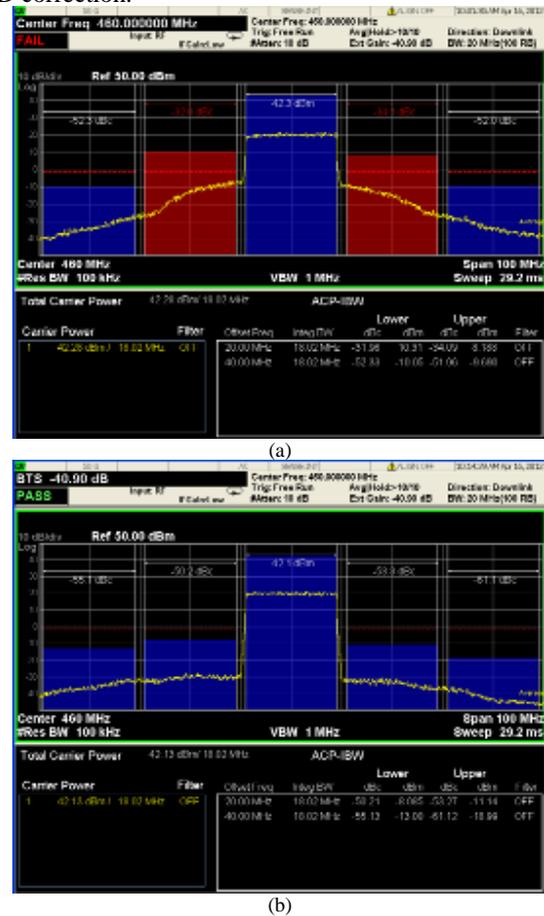


Figure 4. Measured ACLR of the DPA using a LTE-Advanced signal with 20MHz offset at an average output power of 42.1dBm: (a) before DPD linearization and (b) after DPD linearization

Figure 5 shows the measured ACLR of the Doherty power amplifier using a LTE-Advanced signal with 20MHz offset at an average output power of 42.1dBm, and the ACLR was improved from -34.1dBc to -53.3dBc with DPD linearization, meanwhile, a drain efficiency of 48.7% was achieved.

IV. CONCLUSION

A 460MHz unsymmetrical DPA with high efficiency and good linearity for LTE-Advanced applications was presented in this paper. The proposed unsymmetrical DPA was analyzed and the design procedures was detailed. Test with 20MHz LTE-Advanced signal, the proposed Doherty power amplifier shown ACLR of -34.1dBc and -53.3dBc before and after linearized respectively, along with a drain efficiency of 48.7%

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