Research and Design of Beamforming Device of SLC- LSCMA Algorithm Based on FPGA

Qingfang Zhou
School of Physics And Electronic Engineering
Qujing Normal University
Qujing, Yunnan, China
739837379@qq.com

Lei Wang
School of Information Science and Engineering,
Yunnan University
Kunming, Yunnan, China
236530101@qq.com

Yanyan Yu
School of Information Science and Engineering,
Yunnan University
Kunming, Yunnan, China
731496765@qq.com

Jun Yang*
School of Information Science and Engineering,
Yunnan University
Kunming, Yunnan, China
junyang@ynu.edu.cn

***Abstract*—In this paper,we design a uniform circular array beamforming device of 16 yuan based on the least squares SLC- LSCMA algorithm (based on the linear subspace constrained least squares cma) high stability and rapid convergence for the foundation. The design of the complete beam-forming the SLC-LSCMA algorithm by plural, time-multiplier and accumulators, which uses less resources and faster than the traditional algorithm. The beamforming device uses hardware description language of Verilog HDL , and wires on the QUARTUS II 8.0. Finally the beamforming device is downloaded to the Altera's EP2C35F672C6, and its timing simulation can be run properly in the 50MHz clock frequency. This design can be widely used in mobile communication and satellite communications.**

Keywords-FPGA SLC-LSCMA algorithm Beamforming device Smart antenna

I. INTRODUCTION

The smart antenna plays an increasingly important role in today's communication. The beamformer is an important part of the smart antenna. It can adjust the weighting values to control the direction of the function of the antenna array by meeting certain criteria adaptive algorithm to produce a high gain narrow beam, so that enhance the desired signals and suppress the interference signals of the smart antenna. The traditional constant modulus algorithm is based on the steepest descent form algorithm, slow convergence; The SLC-LSCMA algorithm (based on linear subspace constraints of LSCM algorithm) has a fast convergence and low computational complexity, low bit error rate characteristics, that the linearly independent input data can ensure global convergence and stability. The CDMA system is a plurality of constant modulus signal environment of coexistence. The traditional CMA algorithm easily captured other interfering signals, rather than the desired signal. The solution is the use of a plurality of constant modulus array cascade method, but the complexity of this method is quite high. Linearly constrained constant modulus algorithm can solve interference capture problem, but its convergence performance is influenced by the step factor[1]; The SLC-LSCMA algorithm can effectively solve the interference capture problem, and convergence performance is not influenced by the step factor, eliminate the impact of the noise subspace. In this paper, we adopt the FPGA technology, bacause its high level of integration to be completed by the complex timing and combination logic circuit functionality, multiple subsystem functions are integrated into a single chip, the formation of the SOC. Its advantages can greatly reduce the computation time, the antenna beam to meet the real-time fast scan requirements.

II. SIGNAL MODE

Consider a synchronous DS-CDMA communication system having K users. Under additive white Gaussian noise channel, after the chip matched filter and the chip rate sampling, within a symbol interval T, the receiving end of the output samples of an N-dimensional vector:

$$r = \sum_{k=1}^{K} A_k b_k s_k + \delta n \quad (1)$$

Where is the amplitude of the k-th user of the received signal; $b_k \in$ is an information bit of the k-th user of the received signal; $s_k = (\frac{1}{\sqrt{N}})[\beta_0^k, \beta_1^k, \ldots \beta_{N-}^k$ is the k-th user's spreading code vector normalization, $\beta_l^k \in \{\pm 1\}, (l = 1,2, \ldots$ is the spreading code sequence of the k th user; Suppose K users characterized waveforms are orthogonal to each other. If $s \triangleq [s_1, s_2, \ldots,$, $A \triangleq diag(A_1^2, A_2^2, \ldots$, Therefore, the receiving end of the autocorrelation function of the input signal r matrix:

$$R = E\{rr^T\} = \sum_{k=1}^{K} A_k^2 s_k s_k^T + \delta^2 I_N = SAS^T + \delta^2 I_N \quad (2)$$

Eigenvalue decomposition of the matrix R:

$$R = [U_s \; U_n] \begin{bmatrix} A_s & \\ & A_n \end{bmatrix} \begin{bmatrix} U_s^T \\ U_s^T \end{bmatrix} \quad (3)$$

Published by Atlantis Press, Paris, France.

Where $\Lambda_s = \mathrm{diag}[\lambda_1, \lambda_2, \ldots$ is a matrix of K eigenvectors. is a matrix of K eigenvectors. Descending order with the corresponding orthogonal eigenvectors matrix: $U_s = \mathrm{diag}[u_1, \ldots$; $\Lambda_n = \delta^2 I_1$; $U_n = [u_{K+1}, \ldots$ Respectively, represents the the orthogonal feature vector of the N-K. U_s is the signal subspace, U_n is orthogonal parts of the noise subspace.

III. SLC-LSCMA Algorithms Profile

The SLC-LSCMA algorithm constrained by the weight vector signal subspace, so as to eliminate the impact of the noise subspace. The definition is based on the weight of the new signal subspace vector.

$$w = a_1 + B_1 x \tag{4}$$

Where x is the updated weight vector. $B_1 = U_s U_s^T, U_s \in R^{N \times K-1}$ is the zero signal subspace of vector X. x is the adaptive adjusting section of the vector .

In order to get the weight vector w, we must estimate the signal subspace U_s. Projection on S_1 is defined as:

$$Q = a_1 (a_1^T a_1)^{-1} a_1^T \tag{6}$$

Thereby obtaining the projection in the subspace orthogonal to , the reception vector r projection to obtain a new vector to , then of the auto-correlation matrix is:

$$C = E\{r_2 r_2^T\} \tag{7}$$

Eigenvalue decomposition of C as follows:

$$C = [U_s \quad U_n \quad U_0] \begin{bmatrix} \Lambda_s & 0 & 0 \\ 0 & \Lambda_n & 0 \\ 0 & 0 & \Lambda_0 \end{bmatrix} \begin{bmatrix} U_s^T \\ U_n^T \\ U_1^T \end{bmatrix} \tag{8}$$

Among them, $\Lambda_s = \mathrm{diag}(\lambda_1, \ldots \lambda_K$ contains a C in the K-1 the largest eigenvalue; $\Lambda_n = \delta^2 I_1$ value for the characteristics of the noise; Λ_0 ; U_s, U_n and are respectively corresponding orthogonal characteristic component. Compared with the traditional algorithm of LMS and LSCMA, SLC-LSCMA algorithm is not only faster convergence speed, large output SINR, low error rate, and in a dynamic environment can work well [2].

IV. The Design of Beamformer

The purpose of beam forming is reconstructed at the output terminal of the array of the source signal in a certain direction. Different sources exist in the different positions in the space, and these signals are accepted by beamformer. Through adjusting on each element of the right value, we weighted summation of each signal source in the signal space, so that weight adjustment is the core of beam forming[3-6]. Figure 1 is a block diagram of the principle of beam forming.

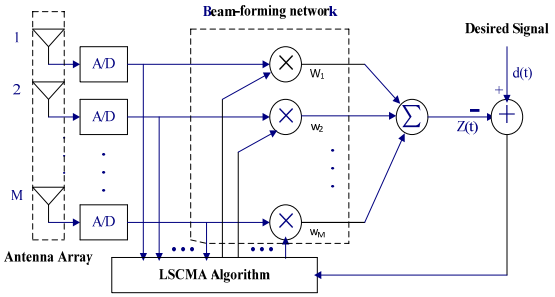

Figure 1. Beamforming schematic

In accordance with the principles of the previous figure, the system output z (t) as:

$$z(t) = w^T x(t) \tag{9}$$

Wherein, A is a weighting vector beamformer. The weighting vector is generally a complex number, which divided into the real part and the imaginary part in the actual use. It is respectively multiplied with a real part and an imaginary part of the signal. In the design, we use FPGA to achieve the SLC-LSCMA algorithm, a complex multiplier, dual-port RAM, shift register and so on.:

A. *The hardware design of the SLC-LSCMA algorithms*

The SLC-LSCMA algorithm is a constant modulus algorithm that does not require the pilot signal and training sequence can be calculated weights and system output. This article is the use of LSCMA algorithm weights to be adjusted and weighted sum. The beamformer uses the SLC-LSCMA algorithm to adjust weighted value constantly and control the antenna array direction function to produce a narrow beam of high-gain. The hardware design of RTL structure of the SLC-LSCMA algorithm shown in Figure 2:

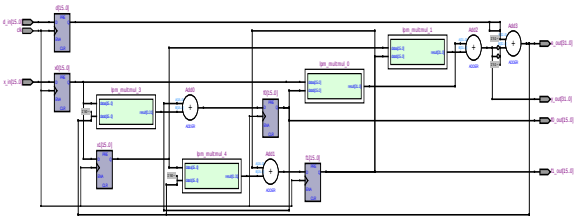

Figure 2. Hardware design of RTL structure of the SLC-LSCMA algorithm.

B. *Complex Cultiplier*

The digital beamformer the way in which the receiver a more detailed block diagram in Figure 3 shows. The i-th array element received the signal $x_i(t)$, through frequency conversion and intermediate level radiation to generate the I\Q dual channel signal $x_{iI}(t)$ and $x_{iQ}(t)$ by the quadrature mixer. Then the two signals respectively become dual-channel digital baseband signasl $x_{iI}(n)$ and $x_{iQ}(t)$ by A / D. This process requires complex multiplier.

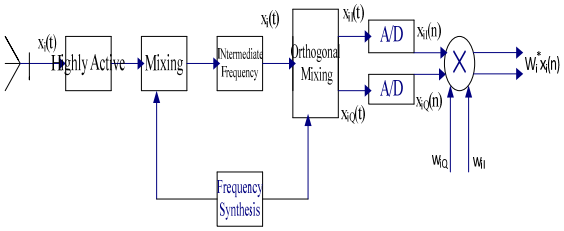

Figure 3. a way of the digital beamforming receiver block diagram

The RTL structure of the complex multiplier shown in Figure 4:

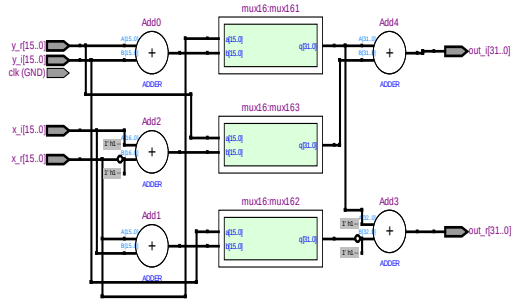

Figure 4. RTL structure of the complex multiplier

C. *The Dual-port RAM*

Coefficient of the output signal of the digital beam profile through the dual port RAM interaction, the weighting factor is written to the corresponding address in the RAM, and then use the beamforming module to read out [4]. In this article, we implement a dual-port BLOCK RAM, which is 32 bit wide, depth 16,with A port read-only and B port write-only. The RTL structure of the dual-port RAM shown in Figure 5:

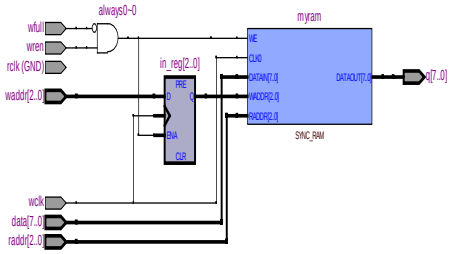

Figure 5. RTL structure of the dual port RAM."

D. *The shift register*

In this paper, we designed a 16-bit register output barrel shifter, for filtering data cache. When the data into in the accumulator and is working, first through the barrel shift register from 0 to 16-bit to circulate and shift left, then calculates. The RTL-level structure is shown in Figure 6.

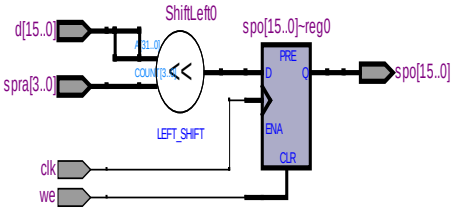

Figure 6. RTL structure of the barrel shifter

V. SYSTEM TEST

In this design, we implement RTL-level description of the digital beamformer by using Verilog HDL language. With Altera's EP2C35F672C6 as target chip, we complete synthesis, placement and routing on the platform of Quartus II8.0. Finally, we use ModelSim SE 6.0 make timing simulation.

Table 1 consolidated results contrast with the literature

Project Name	The SLC-LSCMA guidelines beamformer	Traditional LMS criterion beamformer[3]	LSCMA guidelines beamformer[5]
Occupy logical unit	2649	2703	2697
Computa-tion time	33.874ns	41.376ns	37.259ns

This design in the Quartus II 8.0 can achieve the running speed of 61.4MHz. Compared with the traditional algorithm criteria to achieve beamformer, this design of the hardware resource consumption and computing time there is a certain advantage. The beamformer, compared with the LMS algorithm [7-8], the traditional criteria for the design of hardware resources consumption savings of 2%, 18% increase in the speed of operation. Compared with the literature [9] in LSCMA algorithm guidelines designed beamforming, hardware resource consumption savings of 2%, a 9% increase in the speed of operation. And a high level of integration of FPGA narrowed the the beamformer area.

Guidelines designed to the SLC-LSCMA algorithm beamformer, in the case of the simulation clock is 50MHz, the simulation waveform in Figure 7 below.

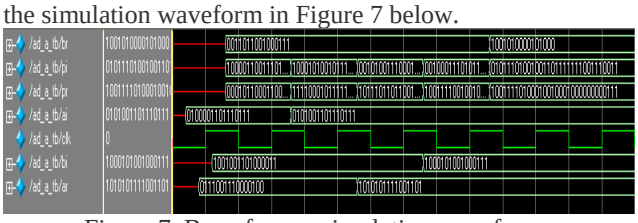

Figure 7. Beamformer simulation waveforms

Analysis of simulation results, enter the four data: ar-1010101111001101, br-1001010000101000, ai-0101001101110111, bi-1000101001000111. Among them, ar, br, respectively for a real part of the input signal and the desired signal; ai, bi, respectively for the imaginary part of

the input signal and the desired signal. Data after the digital beamformer output two data: pr-10011110100010010001000000000111, pi-01011101001001101111111001110011. Wherein, PR and PI respectively for the real part and the imaginary part of the output signal. Consistent results with the results of the the SLC-LSCMA algorithm [10].

VI. CONCLUSION

In this article, we take full advantage of the flexibility of the FPGA internal hardware resources and Verilog HDL language, based on the SLC-LSCMA algorithm, use of the characteristics of high stability and fast convergence of the algorithm, designed to achieve a 16 uniform circular array beamformer. This design enhances the stability and speed of convergence, increased output SINR and BER performance. The design can be widely used in the field of mobile communications and satellite communications.

REFERENCES

[1] ZHAO Li-juan,FENG Guang-zeng. The study of the LSCM algorithm based on subspace. JOURNAL OF CIRCUITS AND SYSTEMS.Vol.15 No.1 pp:21-27 February,2010.

[2] Meng Yan, Wang Jin-kuan, Zhu Jun. A Linearly Constrained LSCM Algorithm Based on Subspace. Journal of Electronics & Information Technology, Vol.31 No.1,pp:49-52, Jan 2009.

[3] YAN Hai,ZHUANG Shengxian,YANG Shuo,ZHUANG Xiaoming. Design of Ultrasonic Array Adaptive Beam-Formed Base on FPGA. Communication & Information Technology .Vol.9 pp:67-69,2008.

[4] QIN Hong-gang,LIU Jing-ke,WU Di. Implementation and application of dual-port RAM based on FPGA. Electronic Design Engineering, 72-74. Vol.18 No.2 pp:72-74 Feb. 2010

[5] TIAN Ke. Design of High Speed and Real2time Digital Beam2forming Processor. Modern Electronic Technique, Vol.18 pp:89-91,2009.

[6] Yan Meng, Jinkuan Wang, Xin Song. Semi-Blind Multiuser Detection Based on Subspace Constrained LMS for MC-CDMA Uplink. The 8th International Conference on Signal Processing [C]. 2006, 3.

[7] Hui Cheng, Shing Chow Chan. Blind Linear MMSE Receivers for MC-CDMA Systems. IEEE Trans. on Circuits and Systems I, 2007,54(2): 367-376.

[8] Enqing Dong, Caihua Zhu, Loretta Evans. Blind Multiuser Detector Based on Reduced Rank Subspace and Least Square Constant Modulus Algorithm [A]. The 8th International Conference on Signal Processing [C]. 2006, 3.

[9] Enqing Dong, Yucai Yan, Peter Parker. Blind Reduced-Rank Multi-user Detector for DS-CDMA Systems Based on Subspace. Asia-Pacific Conference on communications [C]. 2006-08. 1-5.

[10] Y X Chen, W P Zhu, M N S Swamy. A Subspace Constrained Constant Modulus Algorithm for Blind Array. IEEE International Symposium on Circuits and Systems [C]. 2005-05, 4: 3749-3752.

Published by Atlantis Press, Paris, France.