Design for realizing arbitrary fractional divider based on FPGA which duty cycle is up to 50%

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***Abstract*—This paper proposes a novel method for realizing arbitrary fractional divider based on FPGA. Analyzing the limitations of the existing frequency-divided methods, a new model which consists of two-level dividers is put forward. An arbitrary frequency-divided clock output can be obtained by this method approaching 50% of duty cycle. When the division factor is greater than 128, the duty cycle can be very close to 50% of the clock output. This method is proved to be feasible on the FPGA chip of ALTERA.**

Keywords- fractional divider; FPGA; duty cycle

I. INTRODUCTION

In modern communication systems, clock is more and more important as a vital frequency resource. In the system, clocks of different levels are needed in response to equipments of different classes, which need to be correspondingly divided aiming at the system clocks. According to the needs of different designs, we will encounter integer, half-integer, arbitrary fractional divider, etc [Ref.1-5]. Several forms of frequency division appear even in the same design. Generally speaking, the duty cycle of clocks is up to 50%. It is easy to implement when frequency divider ratio is even, while in other cases, it is more difficult [6, 8]. This article, inspired by the design philosophy of the universal half-integer frequency divider, proposes a general design method and achieves the goal of arbitrary frequency of equal duty ratio. With the use of hardware description language of Verilog HDL, development platform of QuartusⅡ9.0 and Altera's FPGA, this article designs a more common fractional divider to fulfill all the above requirements.

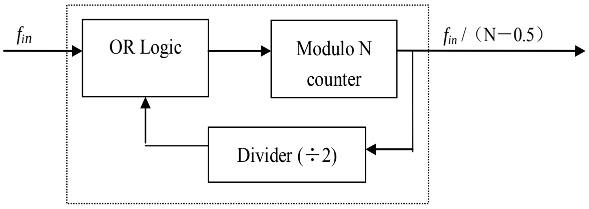

Figure 1. Half-integral frequency divider

Half-integer divider usually consists of a modulo N counter, a divide-by-2 divider and an OR logic, as shown in Figure 1.

The principle can be implemented on the basis of N counters, by means of deducting half cycle of non-frequency clock by Exclusive OR, so as to achieve the N-0.5 count, N-0.5 frequency division and realize that the circuit of deduction is made up of a divide-by-2 divider and an Exclusive OR. Odd frequency (2*N*-1) can be achieved and the duty cycle is up to 50% if the output of the divide-by-2 divider can output signal. It is visible that 50% duty cycle is because of divide-by-2, which can be implemented by a trigger. Based on this, we can construct an arbitrary divider of frequency factor for *K* (as shown in Figure 2), and reach or try to approximate 50% duty cycle.

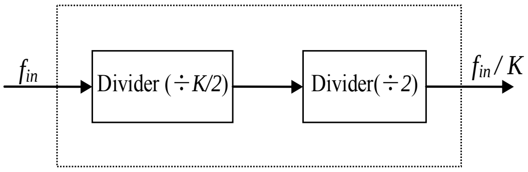

Figure 2. arbitrary divider of frequency factor for K

When *K* takes different numeric values, the *K*/2 divider will appear the situations of an integer divider, half-integer divider and fractional divider. The following are discussed respectively.

II. INTEGER DIVIDER AND HALF-INTEGER DIVIDER

A. Integer divider

When *K* equals to 2*N* in which N is an integer, that is, when *K* is even, *K*/2 divider changes into an integer divider (as shown in Figure 3). Two types of methods can be achieved for the FPGA design of an integer frequency divider. One is to achieve by using a counter, the other is to implement with the use of state machines. The two methods have their own merits. Counter is simple to use and occupies less resource. There may be a number of changes of he outputs of the normal counter, so while using combinational logic to decode the output, because of the issues of signal competition and adventure, the normal counter will cause the peak pulse. Using Johnson counter can avoid the problem, as only one output of it changes under each clock. Sate machines have the advantage of clear levels of description, but occupy more resources. So it can be carefully used in specific designs.

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For an even divider, it can be up to 50% duty cycle, as shown in Figure 3.

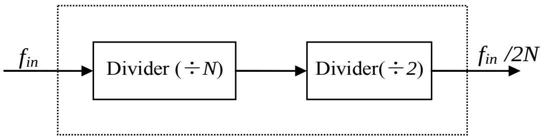

Figure 3. Even divider（K=2N）

B. Half-integer divider

When K equals to 2N-1 in which N is an integer, that is, when k is odd, K/2 divider changes into a half-integer divider (N-0.5).

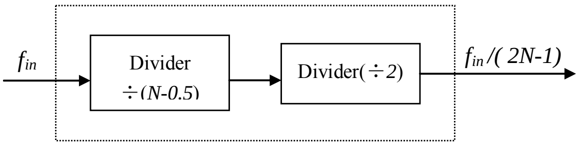

Figure 4. Fig 4 Odd divider（K=2N－1）

Actually we can choose the method as shown in Figure 1, odd frequency signal of 50% duty cycle can be obtained if the output of the divide-by-2 divider can directly output signal. Simulation waveform is shown in Figure 5 in which the wave of outclk1 and outclk2 can be seen in the figure that outclk1 signals producing a rising edge every 3.5 clock cycles achieves frequency of coefficient for 3.5, at the same time, gets a 7 frequency of duty cycle on the outclk2 side.

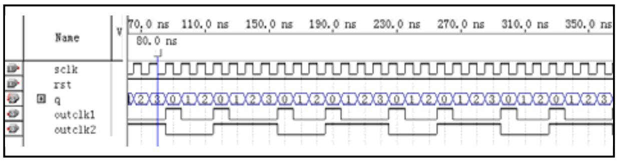

Figure 5. Odd frequency timing simulation diagram(K=2N－1，N=4).

III. FRACTIONAL DIVIDER

When the frequency coefficient K is an arbitrary fraction, K/2 divider is a fractional divider. If K-divided frequency is directly divided, the duty cycle of the output signal varies widely, or deviates more than 50% and is uneven. It can be finally reached K-divided frequency of approaching 50% duty cycle by applying first divided-by-K/2 frequency and again divided-by-2 frequency.

A. Principles of fractional divider

So-called fractional divider is only an averaged effect; the coefficient of every frequency is an integer. Under the effect of the control logic, it is merely switched between the two frequencies. The same as the basic principle of realizing fractional divider, a certain way in several frequency cycles is taken to make a few cycles count more than or less than a number, so as to obtain a fractional divider ratio in overall count cycle of entirely average significance, as shown in Figure 6. Suppose a fractional divider of frequency coefficient for K is to be divided, K can be expressed as:

$$K = \frac{f_{\text{in}}}{f_{out}} = N + \frac{n_2}{n_1 + n_2} = \frac{n_1 N + n_2 (N+1)}{n_1 + n_2} \quad . \qquad (1)$$

In the formula, n_1, n_2, N , are all positive integers. Formula (1) has a clearly physical meaning and implementation methods of engineering. In $n_1 + n_2$ times of dividing frequency, N-divided frequency divides n_1 times, (N+1)-divided frequency n_2 times, and the average effects of $n_1 + n_2$ times of dividing frequency can be achieved to the effects of fractional divider. For example, if you want to get a frequency coefficient of K for 3.7, you just apply divided-by-4 frequency of 7 times and divided-by-3 frequency of 3 times, so the average frequency ratio ＝（3×3+4×7）/（3+7）＝3.7. As another example, K is frequency coefficient for 3.18181818……, that is, when $K = 3 + \frac{2}{11}$, it is enough to divide by 4 frequency of 2 times and divide by 3 frequency of 9 times. The times of divided-by-N and divided-by-(N+1) frequency have nothing to do with the integer portion. For a fractional divider exists two frequencies of divided-by-N and divided-by-(N+1), and each of which divides many times, the two frequencies should be attempted to be mixed well, rather than all divided-by-N frequency over a period of time, divided-by- (N+1) frequency at another time, otherwise, large phase fluctuations will happen. There are two mixed methods:

- The first method:

Step 1: transforming the fractional part of the fractional divider into type of fractional: $\frac{n_2}{n_1 + n_2}$.

Step 2: Each frequency cumulates n_2. If it is less than $n_1 + n_2$, then divides by N frequency, meanwhile, do some adjustments to the accumulated value, minus $n_1 + n_2$, or else divide by (N+1) frequency.

- The second method:

Step 1: the same with step1 of the first method.

Step 2: The accumulated value is set up to n_1 , if is less than $n_1 + n_2$ after accumulation, then divides by (N+1) frequency, otherwise, divide by N frequency. Meanwhile, do some adjustments to the accumulated value, minus $n_1 + n_2$.

The sequence of the frequency coefficient of 3.7 can be realized by using the second method as shown in TABLE I. In the simulation waveform as shown in Figure 6, the duty cycles outclk1 of 3.7 frequency waveform and outclk2 of 7.4 frequency waveform are 50% and 57.1% respectively (average effects approach 50%).

TABLE I. COEFFICIENT SEQUENCE OF 3.7 DECIMAL DIVIDED FREQUENCY

sequence	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
Cumulative results	3	6	9	12→2	5	8	11→1	4	7	10→0
Frequency coefficient	4	4	4	3	4	4	3	4	4	3

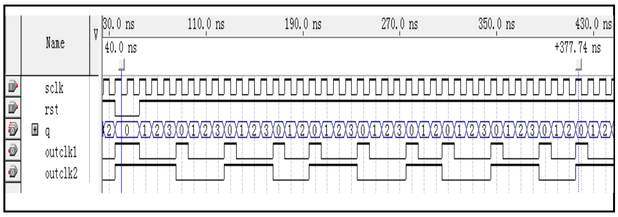

Figure 6. simulation waveform diagram for the coefficient of 7.4 （*K*=7.4，*K*/2=3.7）

B. *The discussion of the duty cycle*

The model of the fractional divider proposed in this article, its duty cycle is changed among $\frac{100(N+1)}{2N+1}\%$, 50% and $\frac{100N}{2N+1}\%$ (*N* is the integer part of *K/2*), and the three values have nothing to do with the fractional part. As the increase of the integer portion *N* of the score coefficient, its duty cycle is increasingly closing to 50%. It can be seen from the TABLE II, when $N \geq 32$, its duty cycle is approximately 50%. The fractional part is only relevant to the average duty cycle. When the fractional part is closer to 0.5, namely, n_1 is closer to n_2, its average duty cycle is closer to 50%. When the fractional part is 0.5, its duty cycle is 50%, that is, $K=2N-1$, and its duty cycle is odd frequency of 50%. From the perspective of duty cycle, this method improves more than bibliography [6].

TABLE II. DIFFERENT FREQUENCY COEFFICIENT CORRESPONDS TO THE DUTY CYCLES

N	1	2	4	6	10	16	32	64	128
duty cycle 1	66.67%	60.00%	55.56%	53.85%	52.38%	51.52%	50.77%	50.39%	50.19%
duty cycle 2	33.33%	40.00%	44.44%	46.15%	47.62%	48.48%	49.23%	49.61%	49.81%

The frequency coefficient K of the arbitrary divider model in Figure 2 must meet K>2. If K is less than 2, that is, K/2 is no longer the frequency coefficient, but the multiplier coefficient. Therefore, It can be dealt with by the following thought that applying phase-locked loop circuit provided by the FPGA chip make it come true. For example, EP1C12Q240C8 chips of Cyclone series in Altera providing 2 PLLs (PLL is the abbreviation of phase-locked loop), module setting method can be used to complete easily. Meanwhile, it can be set with use of digital clock Manager (abbreviated to DCM) in Xilinx's FPGA and analog PLL.

IV. CIRCUIT IMPLEMENTATION AND CONCLUSION

The design method proposed in this article can be realized in Field Programmable Gate Array (abbreviated to FPGA). FPGA chips have the advantages of short development cycle and low cost. It inputs the design logic with the use of EDA technology, hardware description language (VHDL or Verilog HDL) and circuit schematic; downloads and achieves the application specific integrated circuit through simulation, synthesis and adaptation. We used the variety of frequency forms when we designed the laser radar pulse echo signals. The method proposed in this article can realize the arbitrary frequency coefficient, and when the frequency coefficient *K* is greater than 12, the duty cycle is between 53.85% and 46.15%. When *K* is greater than 64, the duty cycle is between 50.77% and 49.23%. When *K* is greater than 256, the duty cycle is quite closer to 50%.

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