ATLANTIS PRESS

*Advances in Engineering Research, volume 178*

Mizoram Science Congress 2018 (MSC 2018)

# State-of-the-art MOSFET and TCAD in the advancement of technology: A review

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The concept of metal-oxide-semiconductor-field-effect-transistor (MOSFET) was proposed by Julius Edgar Lilienfeld and the electrical characterization and mathematical theory began since 1959 at Bell Telephone Laboratories. It has been a revolutionary invention since then and have led to the new generation miniaturized high performance electronics devices like TFET, nano-MOSFETs, FINFET, CNT, nanowire FET, etc. In addition to the rapidly increasing semiconductor industries which have secure significant percentage of the global market, the need to trace back and follow up the progress is quite an essential work which has been carried out time to time. In this work, the historical development of electronics devices, the state-of-the-art MOSFET with the inclusion of threshold voltage roll-off, drain induced barrier lowering and the concept of band-to-band-tunnelling and other such short channel effects (SCEs) encountered in device scaling and emerging novel devices are reviewed, which are believed to be solution of the scaling era as in International Technology Roadmap for Semiconductors (ITRS). In concurrent with the development of technology in various fields the role of technology computer-aided design (TCAD) tools in the advancement of semiconductor industries and originator of such trend have also been illustrated and with the miniaturizing effects encountered by silicon based CMOS technology in the present scenario, researchers have proposed and articulated *The End of the Road for Silicon* or *The Road to the End of CMOS Scaling* foreseeing the current challenges faced by CMOS. Hence, beyond CMOS devices proposed by eminent researchers and ITRS have also been briefly outlined.

Keywords: **Metal-oxide-semiconductor-field-effect-transistor, electronics devices, technology computer-aided design.**

## INTRODUCTION

Semiconductor Industry Association (SIA) representing U.S. leadership in semiconductor manufacturing, design and research, has announced that worldwide sales of semiconductors reached $38.7 billion (World Semiconductor Trade Statistics, WSTS) for May 2018. Hence, the initiation of this revolution in the semiconductor industries can be traced back to the underlying basic concept of metal-oxide-semiconductor-field-effect-transistor (MOSFET) and its geometry were described in J.E. Lilienfeld patents (Edgar, 1930) “Method and Apparatus For Controlling Electric Currents” and “Device for Controlling Electric Current” (Edgar, 1933), which were filed on 8 October 1926 and 28 March 1928 respectively to the United State Patent Office. These patents disclose the concept of field-effect conductivity modulation; but J. Bardeen in his articles “Research leading to Point Contact Transistor” on 19 July 1957 (Bardeen, 1957, 2003; Hoddeson, 1981), stated that the discovery of transistor effect occurred in the fundamental research programme initiated at Bell Telephone Laboratories in early 1946. Thus, essentially the inventions from Lilienfeld, Bell laboratories and Shockley in the invention of the bipolar junction transistor (Shockley, 1952) and all the recent inventions and new ideas are all probably influence directly or indirectly from expansion and improvement of old ideas and experiences and knowledges.

The chronology of advancement in MOSFET and other device can be summarized into three phase;

(i) Discovery phase (1928-1958, first 30 years): This phase really began around 1947, when the basic concept of transistor physics was clearly understood and was

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applied to new transistor structures (point contact transistor) by Bardeen, Brattain and Shockley at Bell laboratories which presented the first working junction gate field effect transistor (JGFET). The milestone discoveries of this phase have been enumerated by C.T. Sah (Chih-Tang, 1988). At the end of this phase, acceleration in development and manufacturing of silicon transistor began in Silicon Valley (Murray Hill, San Francisco) and Shockley's Silicon manufacturing company (1955) acted as a catalyst in the rapid growth. The predecessor of Silicon Valley was started by F.E. Terman (Dean of Engineering, Stanford), when his students - Hewlett, Packard and the Varian Brothers formed the companies bearing their names around World War II.

(ii) Technology development and new device invention phase (1959-1968): This phase was successfully started when thermally grown silicon dioxide ($SiO_2$) was discovered by Atalla, Tannenbaum and Scheibner as a passivation method to stabilize the silicon surface; and

(iii) MOS transistor integration and integrated circuit manufacturing phase (1968-Today): By the invention of monolithic integrated circuit (IC) concept by Noyce and Moore in 1960, this phase was initiated. And the mass production was on the go since 1970 as result of the silicon MOS IC manufacturing company, Intel, which was initiated by Noyce and Moore themselves in 1968 (Brinkman *et al.*, 1997).

In this work, state-of-the-art MOSFET is reviewed with detailing several challenges for nano-MOSFET design. In addition the saturation of device down scaling has been indicated by throwing light to the Beyond CMOS devices in accordance with ITRS report.

## STATE-OF-THE-ART MOSFET

In order to keep up with the increasing demand for miniaturized, low cost, faster products, shrinkage of MOSFET size without any significant fundamental changes in the physics have been the key solution to the semiconductor industries since demonstration of the first MOSFET in 1960 (Brinkman *et al.*, 1997). R. Dennard in 1974 formulated the fundamental principles to scale down device, i.e. if the device dimensions (width, length and gate oxide thickness) including voltages (supply and threshold voltages) are scaled down by the factor of α with increased doping concentration by α, all the electric fields in the scaled transistor remains the same as it was in the original device, hence named "Constant Field scaling". Around the year 2009, as the supply voltage scaling approaches to 1V, this conventional scaling faced difficulty in further lowering the threshold voltage ($V_{th}$) (Brinkman *et al.*, 1997). Aiming to attained high performance faster device and evading the associated short channel effects the state-of-the-art MOSFET can be defined as collision of the following technologies:

(a) Silicon-on-insulator (SOI)/ heterostructure-on-insulator (HOI), technology gain its advantages from the buried oxide (BOX) layer underneath the active silicon layer as shown in Figure 1. This insulator results in the reduction of parasitic capacitances which yield improved switching speed and low power consumption (Fossum, 1993; Tenbroek *et al.*, 1996; Mehandia, 2012)

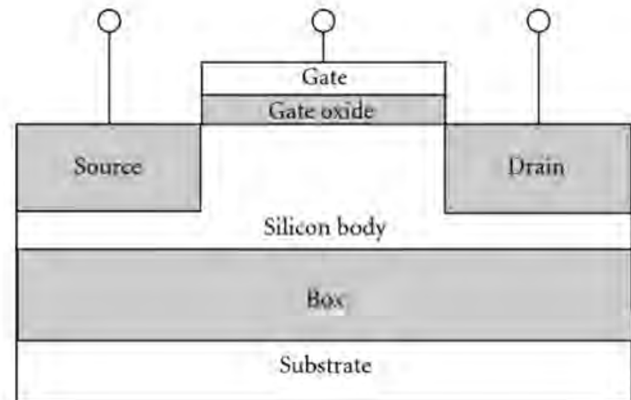


**Figure 1:** Silicon-on-insulator MOSFET (Hu *et al.*, 2002).

(b) High-k/metal gate stack*;* with the scaling of gate-oxide thickness, tunnelling increases which leads to increasing gate leakages. High-k material can be physically thicker without being electrically thicker, which means increased gate capacitance without the associated leakage effects. The main high-k materials used so far are Hafnium silicate, zirconium silicate, hafnium dioxide and zirconium dioxide

(c) Double-gate (DG), triple-gate and gate-all-around (GAA) MOSFETs are the most suitable device structure aimed to increase the electrostatic control of gate over the channel. Figure 2 depicted the structure respectively. As illustrated, compared to single gate MOSFET structure, in double, triple and GAA structure the channel region is controlled and surrounded by gate contacts in different direction, hence the better control of leakage current

(d) FINFET (fin field-effect-transistor) was coined in 2001 by Chemming Hu and colleagues to describe non-planar, double gate transistor built on SOI substrate. The gate is placed on four sides or wrapped around the channel as illustrated in Figure 3. It bears the name Fin-FET due to the fin like structure formed by the source/ drain region.

(e) Strain-silicon MOSFETs evolved with the use of lattice constant mismatch of mainly Si and Ge which result in either tensile or compressive stress which in turn result in band structure alteration and enhanced carrier mobility. As depicted in Figure 4, the conventional strain silicon MOSFET where thin layer of silicon in deposited on relaxed SiGe substrate. Fusion with channel engineering, strain silicon heterostructure-on-insulator device has also recently been demonstrated.

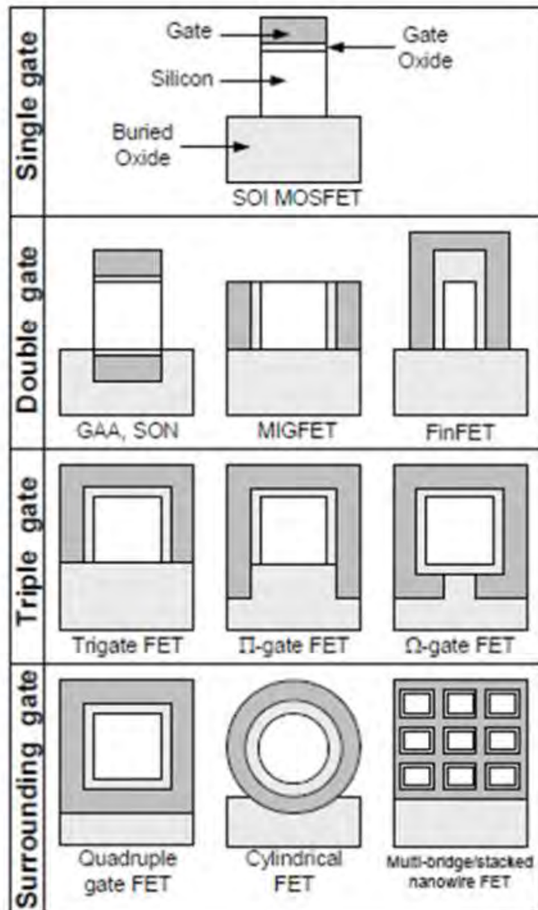


**Figure 2:** Multiple gate MOSFETs (Hu *et al.*, 2002).

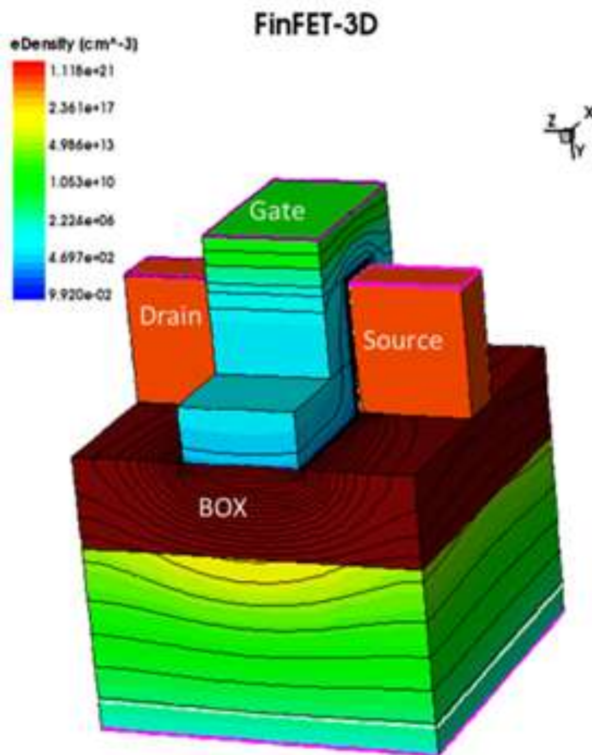


**Figure 3:** Fin-field effect transistor (FinFET) 3D structure simulated design using TCAD.

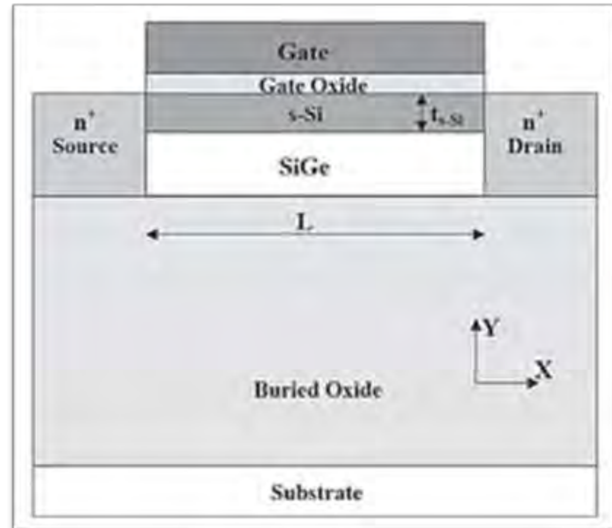


**Figure 4:** Strained silicon MOSFET on relaxed SiGe substrate.

## CHALLENGES FOR NANO-MOSFETS

The major short channel effects (SCEs) of nano-MOSFET which causes design constraints in the recent trends of design and manufacturing in semiconductor industries are briefly illustrated (D'Agostino and Quercia, 2000):

(i) Sub-threshold leakage: The fundamental challenges for nano-MOSFET rooted from the non-scalable characteristics of thermal voltage ($V_T$ = kT/q) which fixated the sub-threshold swing (SS) at constant temperature which is the weak inversion conduction current dominated by the diffusion current flowing between drain and source when $|V_{GS}|< |V_{th}|$, a non-ideal characteristics of MOSFET as a switching device. At room temperature SS is always greater than $2.3V_T$ (~60 mV/dec) which indicates how well the channel surface can be control by the gate. As $V_{th}$ decrease the SS increase exponentially, thus SS must be designed to be as small as possible by using thinner gate oxide thickness (resulting in larger $C_{ox}$) or lowering the substrate doping concentration or lowering operational temperature of the device as SS is a function of T. Furthermore for high performance logic technology, it is required to keep certain level of $V_{DD}$-$V_{th}$ as this determines the drive current which adds to the hurdle of further downscaling (Kim, 2010).

(ii) $V_{th}$ roll-off and drain induced barrier lowering (DIBL): This phenomenon stem from the lowered potential barrier between drain and source due to the relatively increased charge-sharing effect between channel depletion and source/drain depletion regions compare to the long channel device which makes the transistor require less gate voltage to deplete the

substrate beneath the gate dielectric. If the depletion region around the drain continues to extend to source depletion region with increase in drain voltage and finally merge together before junction breakdown occurs, this phenomenon is known as "*punch-through*" which add up to SS leakage.

(iii) Carrier mobility degradation: When the rate of supply voltage scaling is reduced while the geometric scaling rate is the same historical rate, the electric fields inside the MOSFET keep increasing. The drift velocity of carriers is proportional to the longitudinal electric field at low field (<$10^3$ V/cm) after which the increasing rate of carrier velocity decreases with increasing longitudinal field at room temperature and finally reach their maximum velocity when the electric field exceed ~$3x10^4$ V/cm for electrons and ~$10^5$ V/cm for holes. This degradation in carrier mobility is called "Velocity Saturation" (Frazier *et al.*, 1995; D'Agostino and Quercia, 2000; Skotnicki *et al.*, 2005) .

(iv) Hot carrier effects: As the average velocity of carriers in the channel saturates at high electric fields, the carrier can attain high kinetic energy and once they attain sufficient energy to overcome barriers, they might migrate to unwanted area such as gate-dielectric, or substrate. Carrier-injection into the gate-dielectric which causes charges to get trapped in the gate-oxide results in $V_{th}$ shift and instability. And hot carrier near the drain region can generate new electron-hole pair by collision with the silicon atom, known as "*Impact Ionization*" which can increase the substrate current.

(v) Band-to-band-tunnelling (BTBT) leakage and gate-induced-drain-leakage (GIDL) current: when both the source/drain and substrate regions are heavily doped, then BTBT dominates the reverse biased current ($I_{REV}$) as the electric field across the junction increases. GIDL become one of the major components in the state-of the -art MOSFETs. When drain of n-MOSFET is biased at supply voltage and gate is biased at either zero or negative, a depletion region is formed under the gate and drain overlap region and when high electric fields is formed in this narrow depletion region as a result of reverse bias between channel and drain, a surface BTBT current flows through drain to substrate junctions due to twisting of band gaps (Hu, 2009).

## BEYOND CMOS DEVICES

As articulated by ITRS (Carballo *et al.*, 2014) many devices have been proposed in the last 10 years and there are number of nanoelectronic devices that can possibly supplement or replace the current CMOS devices. Some of the listed new devices are more of extension to CMOS and some are of Beyond CMOS most promising devices are (Hoefflinger, 2011; Carballo *et al.*, 2014; Neisser and Wurm, 2015; Courtland, 2016): (i) nanowire (NW) transistor (ii) carbon nanotube transistor (CNT) (iii) graphene FETs (iv) single electron transistors and (v) spin FET (vi) negative gate-capacitance FET (vii) nano-electro-mechanical (NEMS) (viii) all spin logic (ASL). The end road for silicon has been put on the table of discussion and researchers around the world have initiated their works towards it.

## ROLE OF TECHNOLOGY COMPUTER-AIDED DESIGN (TCAD)

Technology computer-aided design (TCAD) tools are used to develop and optimize semiconductor processing technologies and device. Thus, computer (TCAD) simulations and its physical models are used which can be explain to be as the bridge between experimental and theoretical world. It models semiconductor fabrication and device operation. The initiation of commercial TCAD began with the formation of Technology Modelling Association (TMA) in 1979 when research carried out in Stanford which included their famous software program called SUPREM and PISCES under the direction of Dutton and Plummer. Thus, TMA came out with TSUPREM4 and MEDICI, but was later acquired by Avant. Silvaco licensed these programs from Stanford and later offered ATHENA and ATLAS for commercial use. Integrated System Engineering (ISE) being the third vendor of TCAD equipped with equivalent such software called DIOS and DESSIS (Duane, 2002; Fichtner, 2008).

Over the past two decades, TCAD has played a crucial role in device research and technology development as it has branched out into compound semiconductors and novel materials which support a wide range of electronic and optoelectronics devices. In addition quantum phenomena and atomistic effects (Sentaurus, 2012) have been inculcated to support the continued shrinkage of device dimensions. The key advantage of TCAD however relay on the rapid prototyping and ability to analysed the internal physical aspects of the device without having them fabricated on wafer each time for experimental research. This therefore reduced the cost of new devices and pave ways to low cost and faster research in the field increasing the technological development process.

## SUMMARY

Semiconductor industries have grown exponentially with time during the last two decades due to the availability of inexpensive and high performance silicon ICs and of course due to the seamless efforts of many researchers throughout the process. As dimension scaling of CMOS transistors reaches its fundamental limits, "Beyond CMOS" technology have start to draw attention and thus need of the hour. At the same time upgradation of TCAD can essentially ease the path in more sufficient way then it does now. Hence, it is necessary to develop new knowledge and reliability paradigm for nanoelectronics in order to enable

industries to predict design and optimize the device and its performance.

## ACKNOWLEDGEMENT

The authors thank NIT Mizoram for providing blissful facilities and workplace, special gratitude to all the members of Department of Electronics & Communication Engineering for their excellent support throughout the work.

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