A Threshold Voltage Model for the IMOS Device Using Hetero Structure

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Abstract—IMOS allows very sharp subthreshold slopes, even down to a few mV/dec at room temperature. However, the device has serious reliability problems, such as large threshold voltage shifts, caused by hot carrier induced damage and the large supply voltage. Hetero IMOS, using the small bandgap material as the channel material, improves device reliability and decreases power consumption by reducing off-state currents and features a lower breakdown voltage compared to conventional IMOS. In this paper, a threshold voltage model is proposed in different distribution of surface electric field and in the condition of avalanche breakdown. The result is analyzed with the simulation data. It promotes the application of IMOS to VLSI design.

Keywords—avalanche breakdown; Hetero IMOS; threshold voltage

I. INTRODUCTION

While the feature size of MOSFET devices is reaching its physical limits due to several phenomena, such as the high subthreshold swing [1], the thermal diffusion of carriers at low gate voltages and the short channel effect [2], IMOS is receiving an increasing amount of attention. IMOS, proposed for the first by Gopalakrishnan et al. [3] in 2002, is able to reach subthreshold slopes as small as 5mV/dec at room temperature [4]. However, some problems of IMOS, such as the relatively high operating voltage and power consumption, are never ignored due to their negative influence on its reliability. A germanium based device was analyzed by Gopalakrishnan et al. to improve the performance of IMOS [5]. However, there are still many technological barriers to fabricate practical germanium devices [6]. Although a single gate IMOS structure [7], using SiGe-On-Insulator technology (SG-SGOI IMOS) and employing Si1-xGex as a channel material, leads to significant reduction in supply voltages. However, this technique results into an increase in on-state current. Hetero IMOS [7], equipped with with Si/Si-Ge channel, has a lower breakdown voltage, and reduces the operating voltage and power consumption of devices.

In this paper, a model for threshold voltage of Hetero P-IMOS is developed by resolving the 2D Poisson equation and in the condition of avalanche breakdown. By analyzing the model, the reliance of threshold voltage on the drain-source voltage, on the silicon-cap layer thicknesses and on the gate length is studied, respectively. The results of the models are in good agreement with that of simulation.

II. HETERO IMOS STRUCTURE

The basic device structure of the Hetero IMOS is a gated p-i-n diode Fig. 1, as that in the IMOS, except that the channel region employs the Si/Si-Ge channel. In this structure, on top of the Si1-xGex layer is placed a silicon-cap layer. The overall thickness of this layer and the Si1-xGex layer is equal to the thin-film thickness of the device.

III. THRESHOLD VOLTAGE MODEL

The input parameters used for the Hetero P-IMOS are indicated in the Fig. 1. The gate voltage, which leads to the avalanche breakdown, is called the threshold voltage [8]. The distribution of the electric field is firstly analyzed to derive the threshold voltage model. The device is divided into four different parts Area I, Area II, Area III and Area IV. The threshold voltage of the IMOS is controlled by gate voltage and source-drain voltage, so the 2D Poisson should be used to describe the characteristics of Area I and Area II, before the strong inversion appears. The equations in the Area I and Area II can be written as:

\[
\frac{\partial^2 \phi_i(x, y)}{\partial x^2} + \frac{\partial^2 \phi_i(x, y)}{\partial y^2} = -\frac{qN_A}{\varepsilon_{Si}}, \quad (0 \leq x \leq L_d, \ 0 \leq y \leq t_{Si})
\]

\[
\frac{\partial^2 \phi_i(x, y')}{\partial x^2} + \frac{\partial^2 \phi_i(x, y')}{\partial y'^2} = -\frac{qV_A}{\varepsilon_{Si}}, \quad (0 \leq x \leq L_d, \ 0 \leq y' \leq t_{Si})
\]

The potential in the vertical direction in the channel region can be approximated by a parabolic function, the equations are as follows:

\[
\phi(x, y) = \phi_{Si}(x) + c_1(x)y + c_2(x)y^2
\]
We substitute \( \phi_1 \) with \( \phi \) and substituting \( y = 0 \), we obtain the equations:

\[
\frac{\partial^2 \phi_1(x)}{\partial x^2} - a_1 \phi_1(x) + a_2 \phi_2(x) = b_1
\]

(9)

\[
\frac{\partial^2 \phi_2(x)}{\partial x^2} - a_1 \phi_1(x) + a_2 \phi_2(x) = b_2
\]

(10)

We substitute \( \phi_2 \) with \( \phi \), in the equation (9), the result is as follows:

\[
\frac{\partial^2 \phi_1}{\partial x^2} - (q_1 - a_1) \frac{\partial \phi_1}{\partial x} - q_2 \phi_1 = (q_2 a_1 - a_1 b_1)
\]

(11)

In fact, the variation of \( \phi_1(x) \) is enough so smooth that the equation (11) could be simplify as the equation (12):

\[
\frac{\partial^2 \phi_1(x)}{\partial x^2} - \alpha \phi_1(x) = \beta
\]

(12)

We can acquire the solutions:

\[
\phi_1(x) = A \exp(\sqrt{\alpha}x) + B \exp(-\sqrt{\alpha}x) - \frac{\beta}{\alpha}
\]

(13)

The electric field distribution can be written as follows:

\[
E_1(x) = -A \sqrt{\alpha} \exp(\sqrt{\alpha}x) + B \sqrt{\alpha} \exp(-\sqrt{\alpha}x)
\]

(14)

As for Area III and Area IV, 1D Poisson equation will be now applied to determine \( \phi_{s3} \) and \( \phi_{s4} \), we obtain the equations:

\[
\phi_{s3}(x) = -\frac{q N_A}{2 \varepsilon_{Si}} x^2 + C_3 x + D_3
\]

(15)

\[
\phi_{s4}(x) = -\frac{q N_A}{2 \varepsilon_{GeSi}} x^2 + C_4 x + D_4
\]

(16)

The corresponding electric field distribution of the Area III can be written as follows:

\[
E_3(x) = \frac{q N_A}{\varepsilon_{Si}} x - C_3
\]

(17)

In order to determine the unknown element A, B, C and D, the following boundary conditions are used:

\[
\begin{align*}
\phi_{s1}(0) &= V_B \\
\phi_{s3}(L_G + L_{in}) &= V_S + V_{bi} \\
\phi_{s1}(L_G) &= \phi_{s3}(L_G) \\
\left[ \frac{d \phi_{s3}}{dx} \right]_{x=L_G} &= \left[ \frac{d \phi_{s3}}{dx} \right]_{x=L_G}
\end{align*}
\]

(18)

It has been proved that the avalanche breakdown happens firstly in the silicon-cap layer[3]. Therefore, to obtain a model for threshold voltage, we have to find the precise location of the maximum electric field from equations (14) and (17) by substituting the condition \( \frac{dE}{dx} = 0 \). The maximum electric field location will be obtained as \( x_{max} = L_G \). When the electric field in \( x_{max} = L_G \) reaches critical electric field, the avalanche breakdown is triggered, the device is open. By substituting \( x_{max} = L_G \) into (17) and use \( E = E_{cri} \), the threshold model is written as:

\[
V_{th} = \frac{(a_1 - a_2) L_G}{a_2 - a_1} = \frac{q N_A L_G}{\varepsilon_{Si}} - C_3
\]

(19)

\[
E_{cri} = \frac{q N_A L_G}{\varepsilon_{Si}} - C_3
\]

(20)

When we have:

\[
\chi_i = (r_2 - r_1) V_B \exp(\sqrt{\alpha} L_G) + \frac{r_2 q N_A}{\varepsilon_{Si}} (L_{in}^2 + 2L_G L_{in}) - \frac{r_2 q N_A}{\varepsilon_{Si}} \frac{L_G}{\sqrt{\alpha}} = \frac{C_3 r_1}{\sqrt{\alpha}} - \frac{C_3 L_{in}}{r_2} - \frac{r_2 V_S}{r_2} - V_{bi}
\]

\[
\chi_2 = \frac{r_1 \exp(\sqrt{\alpha} L_G)}{\alpha} - \frac{r_2}{\alpha} - \frac{r_2 \exp(\sqrt{\alpha} L_G)}{\alpha}
\]

\[
\phi_{s2} = -\frac{q N_A}{2 \varepsilon_{GeSi}} \frac{L_G}{\sqrt{\alpha}} + \frac{q N_A}{2 \varepsilon_{GeSi}} \frac{L_G}{\sqrt{\alpha}} = \frac{q N_A}{2 \varepsilon_{GeSi}} \frac{L_G}{\sqrt{\alpha}} = \frac{q N_A}{2 \varepsilon_{GeSi}} \frac{L_G}{\sqrt{\alpha}}
\]
\[ \alpha = \frac{a_2a_3 - a_1a_4}{a_1 - a_4}, \beta = \frac{c_2a_3 - c_1a_4}{a_1 - a_4} \]
\[ a_1 = \frac{2 + \frac{2\epsilon_{ox}t_{SI}}{\epsilon_{SI}t_{ox}} + \frac{\epsilon_{ox}t_{GeSi}}{\epsilon_{GeSi}t_{ox}}}{t_{SI}^2(1 + \frac{\epsilon_{GeSi}t_{ox}}{\epsilon_{SI}t_{GeSi}})}, \quad a_2 = \frac{2}{t_{SI}^2(1 + \frac{\epsilon_{GeSi}t_{ox}}{\epsilon_{SI}t_{GeSi}})} \]
\[ a_3 = \frac{2 + \frac{\epsilon_{ox}t_{SI}}{\epsilon_{SI}t_{ox}}}{t_{GeSi}^2(1 + \frac{\epsilon_{GeSi}t_{ox}}{\epsilon_{SI}t_{GeSi}})} \quad a_4 = \frac{2}{t_{GeSi}^2(1 + \frac{\epsilon_{GeSi}t_{ox}}{\epsilon_{SI}t_{GeSi}})} \]
\[ c_1 = \frac{qN_a}{\epsilon_{SI}} - \frac{2}{t_{SI}^2(1 + \frac{\epsilon_{GeSi}t_{ox}}{\epsilon_{SI}t_{GeSi}})} \frac{\epsilon_{ox}t_{SI}}{\epsilon_{SI}} \frac{t_{ox}}{\epsilon_{GeSi}} \frac{t_{GeSi}}{t_{SI}} V'_0 \]
\[ c_2 = \frac{qN_a}{\epsilon_{GeSi}} - \frac{\epsilon_{ox}t_{SI}}{\epsilon_{SI}} \frac{t_{ox}}{\epsilon_{GeSi}} \frac{t_{SI}}{t_{GeSi}} V'_0 \]
\[ V'_0 = V_0 + \Delta \phi_{MIS} \]

**IV. SIMULATION OF VOLTAGE MODEL**

To verify the accuracy of the threshold voltage model, we use Matlab for numerical analysis and use ISE to simulate the model proposed in the previous section.

The parameters used are as following: Work function of gate material $\Delta \phi_{MIS} = 4.6\text{eV}$, $T=300\text{K}$, Drain bias $V_D = 0$, the source/drain/intrinsic doping $N_s = N_d = 10^{20}\text{cm}^{-3}$, $N_A = 2 \times 10^{20}\text{cm}^{-3}$. The results are presented as the following figures.

**Figure 2. Transfer characteristic curve of Hetero P-IMOS**

Fig. 2 presents the transfer characteristic curve of Hetero P-IMOS under different source voltage, including $L_G = L_m = 100\text{\,nm}$. We can easily spot the influence of the source voltage on the threshold voltage. When $V_S$ reduces, the device needs the higher $|V_G|$ so as to attain the critical point of the avalanche breakdown.

**Figure 3. Variation of threshold voltage with Source voltage**

Fig.3 shows the variation of threshold voltage with Source voltage. It can be found that simulation results and calculated results of model agree very well with each other. We can observe that $|V_{th}|$ increases when $V_S$ decreases.

**Figure 4. Variation of threshold voltage with $t_{si}$**

Threshold voltage ($V_{th}$) as a function of the silicon-cap layer thicknesses is shown in Fig.4. By increasing $t_s$, the electric field in the buried channel is decreased. Thus the ionization rate decreases and avalanche breakdown occurs at higher gate voltages. As a result, $V_{th}$ increases.
silicon-cap layer thickness equal to 2 nm is obtained for the structure.

Figure 5. Variation of threshold voltage with the gate length

From Fig.5 we can see that for a given polarization \( V_S = 7.8\, \text{V} \), the threshold voltage \(|V_{th}|\) is smaller for higher \( L_G/L_{in} \) ratios. However, the higher \( L_G/L_{in} \) is, the higher subthreshold slope is. Besides, with a higher \( L_G/L_{in} \), a bigger part of the channel is controlled by the gate. Thus, the ionization rate and avalanche breakdown occurs at a smaller \(|V_{th}|\).

V. CONCLUSION

A threshold voltage model of Hetero IMOS is proposed in this paper. The results of the model are in good agreement with that of simulation. The model in the paper can be easily used for the analysis and design of IMOS so that it is utilized to VILS design.

REFERENCES