Research and Design of Data Transmission System Based on HDMI

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***Abstract*—An improved data transmission system based on HDMI is proposed and implemented in this paper. First, the structure and algorithm of HDMI are discussed and analyzed. Second, according to the audio/video format requirements, a data transmission system based on an improved TMDS codec algorithm of HDMI transmitter and receiver is designed. Third, in order to optimize the internal modules, the encoding algorithm and some internal modules are improved and optimized. Moreover, a color enhanced module and an error correction module are added to the system so as to achieve a better data transmission performance. Finally, the proposed system is implemented using Verilog DHL language and simulated by Modelsim. The simulation results show that the proposed system achieves the functions of data sending and receiving with better performance.**

Keywords-component; HDMI; TMDS; Data transmission; Verilog HDL

I. INTRODUCTION

With the rapid development of technology, electronic display equipments play a more and more important role in our daily work and lives. Clear and fluent images in display equipments are required by more consumers. To display high resolution images, not only high quality of signal source but also the equipment of signal interface with high performance of sending, transmission and receiving of signal are demanded.

With the overall broadcast of high-definition TV and the emergence of digital multimedia devices, there is an urgent need for a higher standard interface to meet the rapid development of high-definition industry. However, the drawbacks of DVI interface become increasingly prominent. The HDMI interface standard came out. In April 2002, total of seven companies including Silicon Image, Hitachi, Panasonic and Philips et al. set up the HDMI organization and developed a new specific digital video/audio transmission standard, namely the HDMI standard.

In view of the current demand for high-definition interface, according to the HDMI specification, in this paper, we optimize the design of HDMI interface. An optimization processing module in data transfer process is added to the system so as to achieve a better application effect.

II. HDMI INTRODUCTIONS

The overall transmission system of HDMI interface includes a transmitter, a receiver, and a data output channel, all of which constitutes three components of signal encoding, transmission and decoding, as illustrated in Fig. 1. The three components include several related modules, such as TMDS codec module, HDCP, DDC, CEC and EDID.

In Fig. 1, audio/video data, and control signal (auxiliary signal, such as the field/line synchronizing signal) are coded and transmitted by HDMI transmitter. In data transmission section, data are transmitted to the receiver through three-way of TMDS(Transition Minimized Differential Signaling) and one TMDS clock channel. Each video pixel can be represented via 24-bit, 30-bit or 36-bit data. The transmission frequency of video data and audio data are up to 165 MHz and 192 KHz, respectively. In data decoding section, audio/video data is received and restored by HDMI receiver, then is displayed at the terminal device.

III. HDMI DATA OPERATION MODLES

According to the difference of data attribute in transmission, the operation modes of HDMI connection can be divided into three cycles including video data cycle, data island cycle and control cycle. In video data cycle, transition minimized differential coding is chosen, thus each channel is coded by 10-bit DC-balanced coding. In data island cycle, data is coded by TERC4, in which 4-bit data is converted into 10-bit for transmission. In control cycle, the 2-bit data (HSYNC, VSYNC, CTL0, CTL1, CTL2 and CTL3) in each channel is coded by transition minimized differential coding.

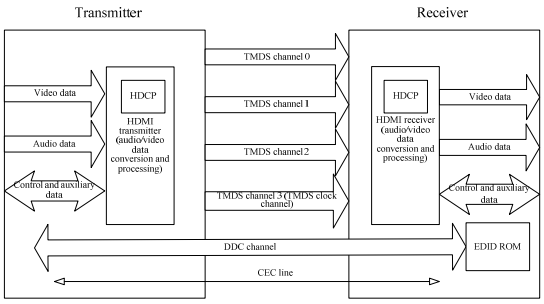

Figure 1. HDMI interface transmission structure

A. *Control Cycle*

Control cycle is mainly used to transmit preamble information at transmitter and synchronize data at receiving end. The control cycle consists of at least seven times of hopping which means data turns from 0 to 1 or from 1 to 0. High hopping of word becomes the basis of boundary synchronization. In video data circle and data island circle, there are up to five times of hopping in the process of data transmission in TMDS codec. Through TMDS coding DC balance is achieved, which is the characteristic of transition minimized differential coding.

The two control signals in each TMDS channel are encoded as follows.

```
case (D1,D0):
    0,0:q_out[9:0]=10'b11_0101_0100;
    0,1:q_out[9:0]=10'b00_1010_1011;
    1,0:q_out[9:0]=10'b01_0101_0100;
    1,1:q_out[9:0]=10'b10_1010_1011;
endcase
```

B. *Video Data Cycle*

Valid video data is transmitted in video data circle. Before transmitting video data, a preamble and two cycles of leading GB are required. During the process of transmission of valid video data after TMDS encoding, the 8-bit data in each channel is converted into 10-bit data of DC balance.

Each 10-bit characters of video data represent 8-bit pixel data. The encoded characters provide DC balance and reduce the 0-1 hopping of data stream. The entire data encoding process can be divided into two parts.

In the first part, original 8-bit data is converted into 9-bit data through minimized differential conversion. The ninth bit of converted data indicates the conversion method. The lowest bit is not changed while other seven bits are obtained by XNOR or XOR with corresponding bits before conversion. What operation model is chosen depends on how to achieve the minimum times of 0-1 hopping, and then the 9th bit indicates the operation model.

In the second part, 9-bit data is converted into 10-bit, then DC balance of entire character stream would be achieved by TMDS characters. The tenth bit indicates in what time the 8-bit data obtained in the first part is needed to be reversed to ensure DC balance. During this process, calculate the number of 0 and 1. If the number of 1 both in transmission data and in input data is more than the number of 0, the code word should be reversed.

C. *Data Island Cycle*

The data island cycle is used to transmit audio data and some auxiliary data, including frame information, description information of valid audio/video data, and description information of data source.

In this cycle, each 4-bit input data is encoded into 10-bit data in each TMDS channel using TERC4. Using 10-bit coding in TERC4 is mainly because its high performance of fault-avoidance that can reduce error rate on the connection.

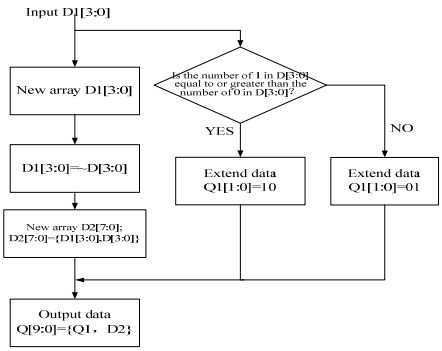

Figure 2. Flowchart of the improved TERC4 coding

Considering the size of final chip, we can encode it using the algorithm coding method. Our method of encoding 4-bit original data into 10-bit DC-balanced codes is as follows: First, reverse original data D[3:0], that is D1[3:0]=~D[3:0]; second, generate new data, D[7:0]={D1,D}; third, expand the 8-bit data into 10-bit. The flowchart of our proposed coding method and the data transmission modes of HDMI are illustrated in Fig. 2 and Fig. 3, respectively.

IV. HDMI TRANSMITTER DESIGN

The structure of HDMI transmitter interface shown in Fig. 4 consists of video capture module including conversion module, audio capture module, audio package generation module, HDCP encryption module and TMDS coding module. Data is sent out after the 10-bit data conversion in TMDS coding module. We can use a configuration register to control the entire run of HDMI transmitter.

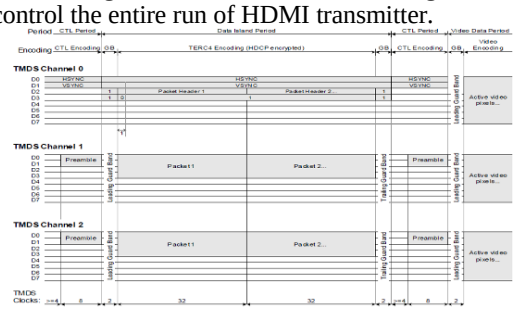

Figure 3. Data transmission modes of HDMI

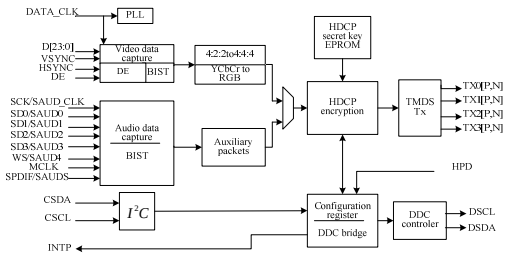

Figure 4. HDMI transmitter interface frameworks

A. *Video Module*

The input signals of video processing module include 24-bit original video data, pixel clock signal PCLK, enable signal DE, and synchronization signal H/VSYNC. Embedded control signal can generate synchronization signal H/VSYNC by itself. The DE generation module defines actual area of video data. By H/VSYNC and clock signal, DE generation module generates DE signal, so that DE signal is not needed to be provided by video decoder. In data island cycle of HDMI, H/VSYNC coding bits are transmitted in channel 0 of TMDS, and in control cycle H/VSYNC signal is transmitted in channel 0 using four different control characters.

In our design, different video formats are transmitted using frequency division and frequency multiplication of clock. When transmitting video data with format of 1280×720@60Hz, the pixel clock can be calculated as: PCLK=1280×720×60=49.3Mhz, and each frame of image has approximately 2.47Mbyte data. In data input buffer area, synchronization control signal controls data reading and writing. When each VSYNC high level comes, the controller clears write-in address data in buffer. When the DE level becomes high, the write-enable signal is set high and the data write function starts to work, at the same time write address is added one once the PCLK plus comes. When DE level becomes low, write enable signal is invalid and operation is stopped. In this way, under the control of buffer area, the 24-bit pixel data is cached in order to ensure the integrity of video data. Fig. 5 shows the simulation results of one-bit data in write cache controller. In overall design, while loop is used to read out the 24-bit data in buffer.

B. *Audio Module*

Using S/PDIF interface to transmit audio signal is a common method. When data comes into HDMI, we need to encode the received data. First, recognize the preamble of received data. Second, determine the data frame configuration. Third, encode data into packets and output them. The structure of audio module is shown in Fig. 6.

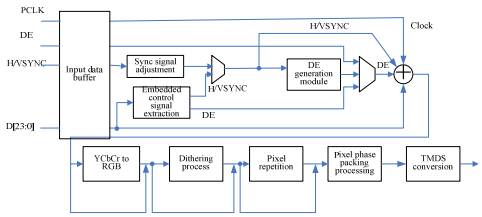

Figure 5. Structure of HDMI video module

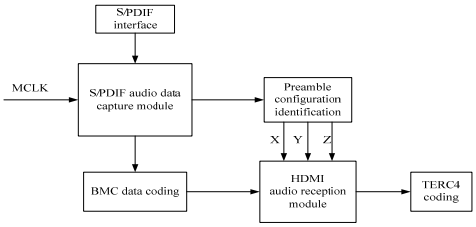

Figure 6. Structure of HDMI audio module

C. *Simulation and Implement*

Here, we make the simulation in a single TMDS data channel as an example. The input data includes video, audio and control data. The simulation results are shown in Fig. 7. As clearly seen from Fig. 7, the coding of entire data performs strictly according to HDMI standard.

When vde=1, video data is valid. We have mentioned above that there is a guard band before the start of audio/video data cycle. From the waveform in Fig. 7, we can see that dout=10'b1011001100 in output terminal is the start of video data guard band. After two guard band, video data is started to be transmitted. The transmission of audio data works in the similar way.

V. DESIGN AND IMPLEMENT OF HDMI RECEIVER

Though there are variety of HDMI receivers, the structure of them are much the same. Overall, reception of HDMI is the reversed of transmitting. In this section, we discuss the dual HDMI ports to illustrate the modules structure of HDMI receiver shown in Fig. 8.

A. *Clock Generation and Synchronization Simulation*

TMDS receiver must have a phase lock, and a series of clock signals including pixel clock, reference clock and sampling clock. In our design, by PLL circuit, the phases of coding clock and sampling clock are directly locked in pixel clock. So even if pixel clock jitters slightly in transmission, the sampling module can obtain almost the same relative phase difference between clock and code element.

In receiver, the sampling clock is divided into several clock signals with different phases. Using this method to sample symbol signal then pixel data can be exactly recovered, and synchronization control signal is obtained.

As shown in Fig. 9, we use a PLL to perform clock synchronization and phase locking. When LOCKED=1, clock information is locked to the frequency of CLKIN and output clock is valid. We also use PLL to perform the 1/2 frequency division, 1/4 frequency division and frequency doubling on input clock signal. The output clock is delay with respect to timing sequence.

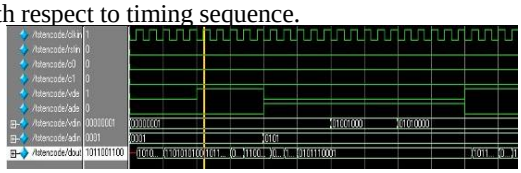

Figure 7. Simulation of HDIM transmitter

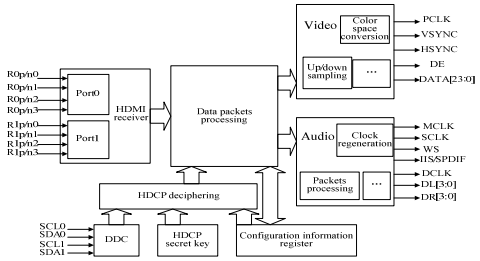

Figure 8. Structure of HDMI receiver module

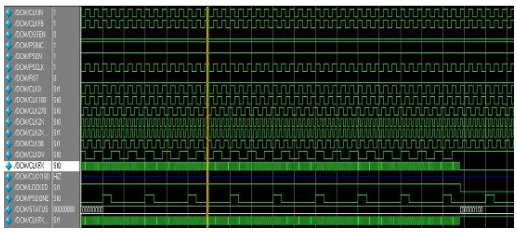

Figure 9. Simulation of HDMI receiver PLL

B. *Internal Module Design of HDMI Receiver*

The video processing in receiver as shown in Fig. 10 is mainly the same as transmitter, including up/down sampling, color space conversion, and pixel dithering processing.

C. *Implement of Receiver Using Verilog*

According to the architecture of HDMI receiver module, we implement the receiver using Verilog HDL. The simulation results of HDMI receiver are shown in Fig. 11. The clkin is input reference clock and also the data acquisition clock. The tmdsclk_p/n is TMDS clock cycle, and equals to pixel cycle. The cycle tmdsclk is 5 times the cycle of clkin using double-edge data detection. The re1_p/n、re2_p/n、re3_p/n are three acquisition channels of TMDS differential data. The vde and ade are enable identifies of video cycle and audio cycle, respectively. The hsync/vsync are line field signal. The sdout are 30-bit transmission data, in which the data size in each channel is 10-bit. The aux1/2/3 are audio or auxiliary control data, working when ade = 1. The re1/2/3 are three components of video pixel after decoding of the three TMDS channel data.

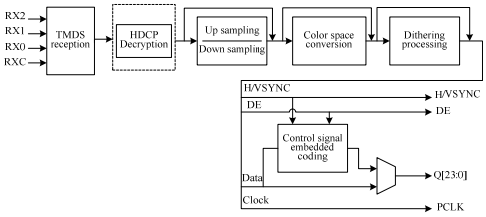

Figure 10. Structure of HDMI receiver video processing module

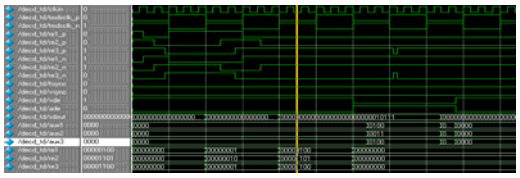

Figure 11. Simulation of HDMI receiver

VI. CONCLUSIONS

HDMI transmitter and receiver are design and implemented as well as simulated using Verilog HDL in this paper. The data jitter processing module, data island codec module and receiver error recovery are design and implemented. The functional simulation results by Modelism show the correctness of the transmission system in framework and on function. The experiments demonstrate the feasibility of the design.

ACKNOWLEDGMENT

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