A New Synchronization Method Based on SDI with Variable-Length Frame

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Abstract—**The Serial Digital Interface is widely used in high sp eed uncompressed video data transmission.It's unsuitable to us e the clock recovered from original data as the reference clock, because the recovered clock has large clock jitter. It must have low enough jitter. Traditionally, offset compensation and drift compensation are used to achieve time synchronization.In this paper, a new mechanism to synchronize time by changing the Frame structure is carried out. This mechanism avoided introducing the extra hardware by changing the frame's structure.**

Keywords-FPGA;SDI;Clock Synchronization;Clock Jitter; clock skew

I. INTRODUCTION

With the development of broadband wireless communications technology,the HD video wireless transmission systems has become one of the research hotspots.

For the clock jitter and skew, the data transmitted between SDI and FPGA equipment would become redundancy or discontinuity. At present,experts have put much effort in resolving clock synchronization by PLL (Phase Lock loop, a phase-locked loop clock synchronization method of [1-2]).It's said that PLL is one of the most effective methods to track phase and frequency.But it could not acquired the requirements of clock synchronization for uncompressed burst data quickly. Furthermore, traditional synchronization technology ,such as GPS,SDH/PHD,all required expensive and high precision crystal oscillator[3].Recently, most of researches interest in the complicated algorithm,such as RBS, DMTS[4], FTSP, AD[5], TPSN, TS/MS, LTS[6]etc. .Most of them put much effort on how to compensate the clock offset,but not interest in the resolving the drift.To resolve it ,a "reservoir"method is proposed In [7].But it need a buffer memory deep enough.As the OFDM_MIMO system is considered,this buffer memory would waste much resource.So the target of our study is to find a resolution to eliminate the clock jitter and skew without additional hard ware and with fewer resource.

The clock synchronization is achieved by changing the structure of the data frame.It just need two counter and a few other resources to calculate the deviation between two asynchronous clock. To synchronize the frame, it need't correct the clock which has jitter or skew,but only change the frame structure according to the deviation.It's very suitable for processing the clock synchronization between FPGA and SDI interface.

II. THE SYSTEM STRUCTRE AND DESIGN OF CLOCK

A. *Video interface of SDI*

SDI is widely used in the studio digital television equipment,which is formulated by the American Society of motion picture and Television Engineers (SMPTE).It is used to transmit unpressed vidio/audio data by a single coaxial cable.At present, there are mainly 3 kinds of formats: SD_SDI, HD_SDI and 3G_SDI. The corresponding data rate were 270Mbps, 1.485Gbps, 2793Gbps. In this paper,we use HD_SDI interface.SDI interface is not like parallel interface that uses a separate data transmission clock signal, its clock is recovered from data signal.

B. *The transmission and data structure of SDI*

The system transmit video data with the modulation and channel coding technique that combined 4*6 MIMO and OFDM with 2048 sub_carrier.At the transmitter one serial SDI single transform into 4 parallel signal and recovered the clock.Then every signal transmit out before been modulated by RS code,64QAM,MIMO,OFDM etc.The receiver demodulation them correspondingly. Based on IEEE 802.11n standard protocol,the structure of the data frame is formed by short training sequence(AGC),long training sequence (LTF),OFDM symbols,cyclic prefix and the tail.The tail formed by a string of "0"whose length is variable.This frame structure is shown in figure.1.

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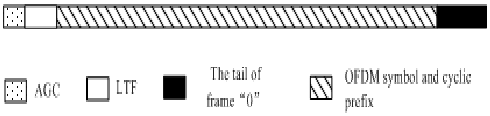

Figure 1. The frame struct of the transmited data

In the SMPTE 292M standard, HD_SDI interface data rate is 1.485Gbps. The video data code by RS code(870,710) based on G(12)and modulated by 64QAM，so every OFDM symbol actually equal to 8520 bits data and the processing clock is 120MHz.

III. THE DESIGN OF CLOCK SYNCHRONIZATION

A. *The jitter in Data*

In practical application, the different physical and chemical properties between different units,resulting in the data rate with different delay. There isn't a signal for clock transmission between SDI and FPGA,So the clock recovered from the data get the same clock skew. Besides ,the FPGA local clock itself has a certain clock jitter,witch will increase the deviation between the local clock and the clock recovered from SDI data. If the skew rate can't be controlled within the acceptable range, it will influence the quality of video image restoration, or even make the image loses lock.

B. *Design of synchronization system*

As the HD_SDI standard data rate is 1.485Gbps, the frequency offset is 1000ppm. While the FPGA local clock jitter just float from 10 to100 ppm. So we analysis this system without consideration the local clock's jitter. As described before,the local clock is 120MHz.In order to synchronize the serial 1.485Gbps data and the four parallel 120Mbps data,we fill the end of each frame with variable length of "0",but not change corresponded clock as traditional method.

Actually,the target of this design is to ensure that the time cost by input data transmission and by output data transmission are equality. It is controlled by adding "0" or reducing "0" at the end of frame.This is shown in figure.2.

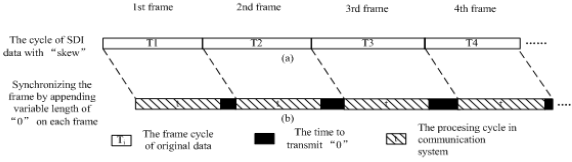
1st frame
2nd frame
3rd frame
4th frame
The cycle of SDI data with "skew"
T1
T2
T3
T4
(a)
Synchronizing the frame by appending variable length of "0" on each frame
t
(b)
Ti
The frame cycle of original data
The time to transmit "0"
t
The procesing cycle in communication system

Figure 2. The frame struct schematic of clock synchronizaton at transmitter

As shown in Figure.2, we compensate variable length of " 0 "at the end of the frame, so that the data can be transmitted continuously and correctly. As the figure.3 (a) shows , the FPGA input data which is received from SDI interface have great "skew",so that the time cost by each frame period is not equal. In Figure. 3 (b) , the t expressed the time cost by transmitted in 120MHz. For this local clock is stable, the t is equal in each frame.The black block present the variable length of "0"to ensure that each frame has a same cycle corresponding to each frame in the figure.3 (a) .

At the receiver, in order to demodulate correctly, the number of " 0 "that must be removed is calculated by DDS, according to the transmitter. As shown in figure 3.

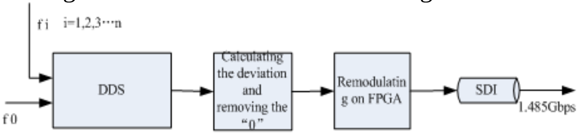

Figure 3. The schematic of clock synchronizaton at receiver

In this paper ,we focus on how to implement the clock synchronization module in transmitter.

IV. THE IMPLEMENTATION AND THE SIMULATION OF SYNCHRONOUS SYSTEM

A. *The principle of implementation*

The serial data received from SDI ,whose data rate is ±1.485Gbps with big "skew" ,are converted to a new signal,whose width is 20bit and rate is ±74.25Mbps. In this paper, we set the clock recovered from this signal as Ft and the local clock as F0. The mathematical model is shown below:

$$\frac{n_t}{F_t} = \frac{n_x}{F_0} \qquad (1)$$

Where n_t represent the number of data in a frame with data rate at F_t .And n_x is to F_0, what n_t is to F_t . For the n_t and F_0 are constant, the n_x changes along with F_t whose clock jitter is less than 1000ppm.The bigger the n_x is,the longer string of "0" is. For example, if F_t is 74.25MHz, corresponding to that n_x=n_0.If the Ft has changed, then the number of "0" obtain by equation (2). If the n_x is greater than n_0 ,more n "0" would be appended . otherwise, less n"0"would be appended.

$$n = \begin{cases} n_x - n_0, n_x \geq n_0 \\ n_0 - n_x, n_0 \geq n_x \end{cases} \qquad (2)$$

Coming to a conclusion, the number of "0" appended , actually,is decided by the deviation between the F_t and the 74.25MHz.The transmission rate of "0" is $F_{0,}$So we design two counter whose clock corresponding to F_0 and F_t, in order to calculate the deviation between the two clock. The implementation of transmitter is shown as Figure.4.

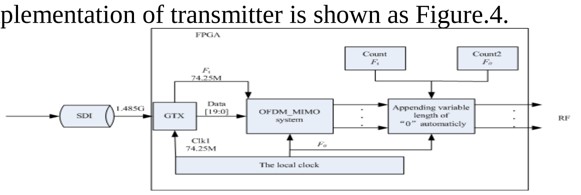

Figure 4. The schematic of clock synchronization at transmitter

B. *The results of simulation*

In order to simulate the"frequency drift" in practical scene, we change the input clock(F_t) from 74.17575MHz to 74.32425MHz. These boundary value are calculated by the ±1000ppm when the standard value is 74.25MHz.Based on the MIMO_OFDM model described in chapter 2,the local reference clock is 120MHz(F_0).In simulated program, there are 38432 data form the head of a frame(AGC+LTF) and

2648 data form a symbol of OFDM,including 600 cyclic prefix.Each frame has 512 OFDM symbols.

The n_x is obtained from equation (1) and the known parameters that mentioned above. So the number of “0” equals n_x-512× 2648-38432.In order to check the result when the frequency drift from -1000ppm to +1000ppm.In this paper, we choose -1000ppm,0ppm,+1000ppm as the clock skew to simulate.That is to say the frequency of F_t is corresponding to 74.17MHz,74.25MHz and 74.32MHz. Their simulation result are shown as Figure.5,Figure.6 and Figure.7.

Drawing a conclusion, if the input frequency (F_t) changed from 74.17MHz to 74.32MHz，the number of “0” appending to the end of frame change from 14363 to 17212. Then, the problem of clock synchronization resolved quickly.

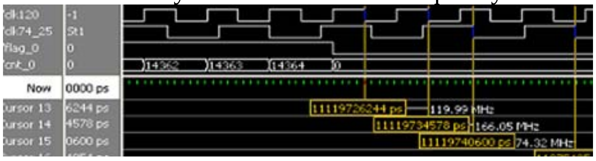

Figure 5. The simulation result of positive jitter

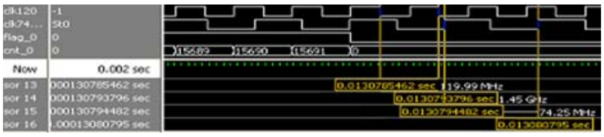

Figure 6. The simulation result when inputted data without jitter

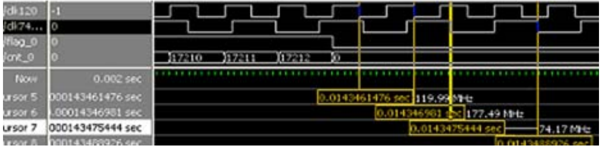

Figure 7. The simulation result of maximal negative jitter

C. *The comparison of results*

For ease of comparison, we built another MIMO_OFDM experimental platform, which the number of “0” appended is not variable.That is to say the frame structure is fixed. Compared with this study, the different error rate between the two system is shown in Figure .8.

The simulation results show that, in the absence of clock drift and jitter of the case (clk=74.25MHz), the two system performance no difference.But in the system whose frame is fixed,the error rate increasingly higher ,along with the increasing of clock skew.And in the system reserched by this paper, the error rate almost increased nothing,when the clock skew growing.

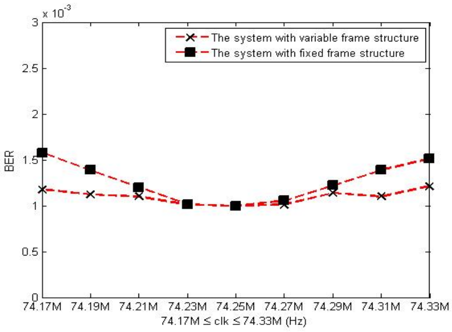

Figure 8. Figure 8.The error rate between fixed frame and variable frame structure

V. CONCLUSION

This paper designed a SDI interface frame synchronization method on the FPGA.Based on the frequency deviation between two clock,it implemented the frame synchronization by changing the structure of the frame. Compared with traditional algorithm, this method need’t explicitly calculate the clock jitter and skew,even need’t big buffer memory.Without additional hardware,this method saved hardware resource and has the good reference value for the engineering practice.

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