The FPGA Implementation of Pulse Wave Feature Extraction

Dejun Guan, Li Lin
Shenyang Radio and Television University
Shenyang, 110003,China
E-mail:Sunbaby20051001@126.com

***Abstract*—Pulse wave signal is analyzed in this paper especially the type I smooth pulse is selected to be further discussed. CPU is designed by using FPGA chips. This CPU contains various IP cores' components, and can carry out multiple calculations and driving peripheral function. This paper implements the extractions the feature points of the specific pulse waves by using the CPU. The result of the design is basically ideal and achieves the expected target.**

Keywords-Pulse Wave; Feature Extraction; Wave Restore; FPGA; SOPC

I. INTRODUCTION

In medicine, the pulse signal is mainly used in pulse checking of traditional Chinese medicine. Pulse wave signal analysis based on FPGA can be used in remote medical treatment. With the development of science and technology, human demands are extended, and traditional Chinese medicine is taken more and more seriously. However, excellent Chinese medicine doctors are of very limited quantities in China and even in the world, and are centralized. Pulse signal transmitting technology can make traditional Chinese medicine more extensive, be more accurately applied to health care, and remove these patients burden of seeing doctors. Pulse signal transmission can solve these problems. With the help of remote consultation system, network communication technology and patient information systems, middle and long distances' Chinese medicine interrogation will be realized [1].This design is to realize one part of pulse transmission technology in telemedicine. Pulse transmission technique is to collect patients' simulation pulse signals, and converts them into analog signals by means of storage, compression and transmission (digital signal). Then doctors can diagnose the patients in a certain distance [2].

II. RELATED TECHNOLOGY

A. FPGA Technology Overview

FPGA refers to Field Programmable Gate Array, namely the field programmable gate array. FPGA uses LCA (Logic Cell Array) concept, including CLB (Configurable Logic Block), IOB (Input Output Block) and Interconnect three parts. ASIC circuit is designed by FPGA. The users does not need to put them to production, but can get operable chips, which can be used as pre-production samples in other full-custom or semi custom ASIC circuit. FPGA has rich trigger and I/O pin. It is one of the devices with short design cycle, minimum development cost and risk ASIC circuit. FPGA adopts high speed CHMOS technology, which is of low power consumption and is compatible with CMOS and TTL level. That is, FPGA chips are one of the best choices in small batch system to improve system integration and reliability[3].

B. EDA technology and Quatus II software application

EDA is electronic design automation. EDA technology takes computers as tools. The designer uses hardware description language HDL to complete design documents in EDA software platform. Then the computer automatically completes the logic compilation, simplification, segmentation, comprehensive, optimization, layout, wiring and simulation, until adaptive compile, logistic mapping and programming download work of the specific target chip [4].These devices can reconstruct hardware structure and working way through software program, so that the hardware design can be as fast and convenient as software design.

C. SOPC technology and Nios.II software applications

1) An introduction to SOPC Technology

SOPC technology is a system on programmable chip, which is based on the large scale FPGA chip system. SOPC design technology is highly developed product of modern computer aided design technology, EDA technology and large-scale integrated circuit technology. System on programmable chip (SOPC) is a special kind of embedded system: first of all, it is a system on chip (SOC), that is the completion of the system main logic function by a single chip; secondly, it is a programmable system, having flexible design, downsizing, extensible, upgradable, and with software and hardware in system programmable functions. A SOPC system includes at least one embedded processor core, and has a small capacity in high speed RAM resources [5]. SOPC system is based on IP core system, so basic knowledge of IP nuclear resources must be grasped in SOPC development. The SOPC system has enough on-chip programmable logic resources, a processor debug interface and FPGA programming interface, which may also contain a portion of the programmable analog circuit. It has characteristics like single chip, low power consumption and micro encapsulation.

The switch and the LED program are used to describe SOPC technology use, SOPC system development method and Nios II software application methods.

2) SOPC technology software control design

After CPU setting, CPU function still needs to be described in Nios II software. The main process this procedure implements is shown in Figure 1.

Published by Atlantis Press, Paris, France.

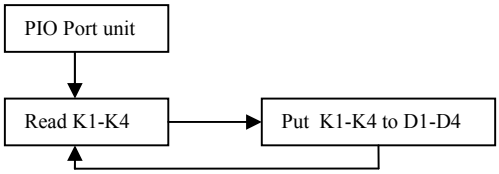

Figure 1. Program flow chart

As you can see, this makes use of IORD_ALTERA_AVALON_PIO_DATA () function and read input PIO port status. And IOWR_ALTERA_AVALON_PIO_DATA () function is used to assign Output PIO port. At the beginning of the program, Button_ISR_Init (void) function must be called for PIO nuclear initialization, otherwise the program doesn't respond.

After compiler running, when the four switches are set to different values, the brightness of LED lamp in response would change.

III. The Principle And Design Of Pulse Wave Signal By Using FPGA Technology

All experiments and results are based on ALTERA's Cyclone II series chip, which chip model is EP2C35. The development platform of experiment is EDA/SOPC experiment development system developed by Beijing Encyclopedia. The peripheral resources of experimental system include several major modules such as interface communication, control, storage, data conversion and man-machine interactive display. The main module includes SPI interface (to achieve read AD and DA output data communication), serial ADC/ DAC (achieve A-D / D-A conversion), 8 keys (the realization of the regulation of feature points), a simple analog signal source (provides an interrupt signal), a clock module (providing a clock signal) and the LCD display screen (show the digital quantity and extraction interface of feature points).

Pulse wave feature points extraction mainly includes two parts: (1) extracting the four feature points of a pulse wave; (2) displaying the characteristic points in the LCD screen.

Pulse sequence reduction is conducted to the given pulse wave point characteristics which mainly include four parts: (1) key press response; (2) AD/DA conversion; (3) LCD screen display; (4) fitting calculation.

Pulse wave characteristic point extraction mainly includes two items: (1) extracting the five feature points P1, P2, P3, P4, P5 of a pulse wave; (2) mark the five feature points in the LCD screen.

Because there are many pulse wave types, the main purpose of this design is not the theoretical research of various waveform feature points, but to realize the feature point extraction with FPGA devices. Therefore, here we only extract the first pulse wave feature point.

Human pulse wave is complex. One of the reasons is that each cycle is not the same. The feature point types in one cycle are not consistent with other cycles. On the other hand, some patient's pulse wave is particularly evident. To identify the feature points of each cycle, each cycle of pulse wave must be identified. Therefore, the first step of pulse wave feature point identification is the cycle identification [6].

The current waveform recognition methods are mainly the frequency domain identification method of wavelet transform, threshold method, the contour constraint method, area method, digital filtering, syntactic method and slope method. The frequency domain identification method of Wavelet transform is suitable for non-stationary pulse signal feature extraction method. It requires each signal decomposed into 5 layers, and extract every scale's wavelet coefficient. According to the equivalent relationship between wavelet coefficient and signal energy, the normalized each wavelet coefficient energy value is set as the feature vector of pulse signal recognition. Pulse signal spectrum characteristics are combined with the experimental data. The improved energy feature vector got from statistical analysis is used to distinguish cardiovascular disease and normal people's conclusion with limited samples. The threshold method is to respectively determine the upper threshold value and the lower limit of the location of the feature points, then extract further the feature points in the threshold.

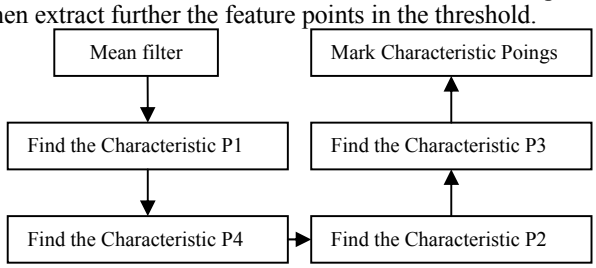

Figure 2. Threshold method feature points flow chart

According to the characteristic of pulse wave and FPGA, threshold method is more appropriate to be adopted[7]. It can be seen that recognition algorithm is simple and flexible in practical application. Specific threshold method process is illustrated in Figure 2.

There are many kinds of filtering method, including wavelet transform filter, FIR filter, IIR filter and time domain filtering. Here we use time domain filtering method. Time domain filtering is composed of intermediate value filter and the average filtering method. While selecting filter method, Matlab simulation software is adopted to simulate. The followings are the results: Figure 3 (a) is the results produced by a 50 point filtering median filtering method. Figure 3 (b) is the results of a 50 point filter mean filter method. So a flat slope will be produced in a peak from median filtering method. While the actual pulse wave should be a smooth curve, so the filtering effect is not ideal. So we further adopt mean filter method. Further simulation experiments are done on the point problem. Figure 4 (a) is the results of 5 filtering. Figure 4 (b) is the results of 20 filtering. Figure 4 (c) is the results of 50 point filter results. We can see that the results of 5 point filter are not smooth, but 20 points result has been more greatly improved than that of 5 points. The effect figure of 50 points is not greatly different from that of 20 points. For efficiency and memory occupation, multi-point filter is unfavorable. Therefore, we selected 20 point mean filter method.

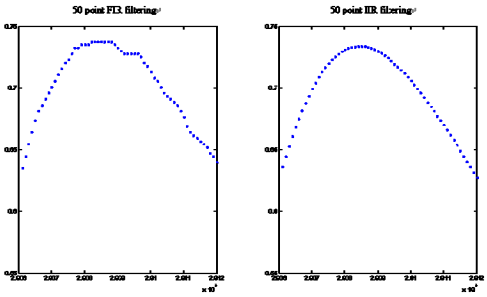

Figure 3. Comparisons between median filter and mean filter (20 point)

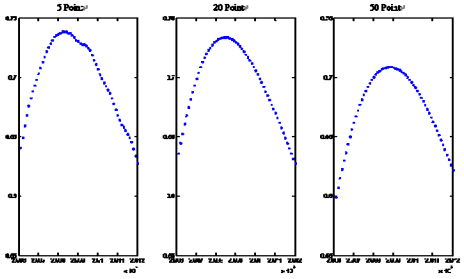

Figure 4. Mean filter comparison of 5 point, 20 point, 50 point

Search period mentioned above is a very important step. Cycle recognition method requires the use of the threshold value method. The threshold method is based on experience. Firstly find the maximum and minimum values of all values and then take the 1/4 distance of maximum value from the maximum and minimum values and extract the region greater than it in each cycle. See Figure 5. The average of the difference between the starting points of each region is the cycle length.

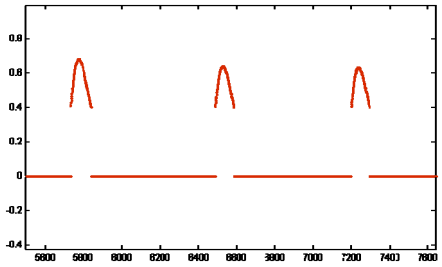

Figure 5. Pulse wave region of signal value greater than the threshold

The average cycle pmean formula can be seen in Figure 4.1.

$$pmean = \frac{1}{n}\sum_{1}^{n}(a_{m+1} - a_m) \tag{4.1}$$

Four feature points can be identified after finding the cycle. The method of looking for feature points P1 is in search of a maximum value in each of the above areas. The maximum point is that all P1 points. Then cycle from an to bn. If the next number is greater than the highest point value, it is set to the highest point; if less than it, the highest point won't change. Finally get the highest point P1in each cycle. See figure 6.

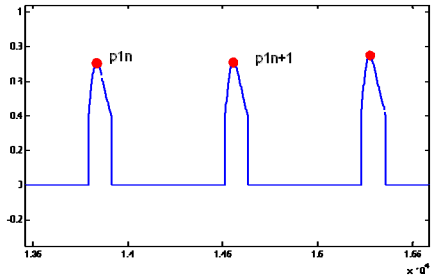

Figure 6. Waveform graph of extraction maximum P1

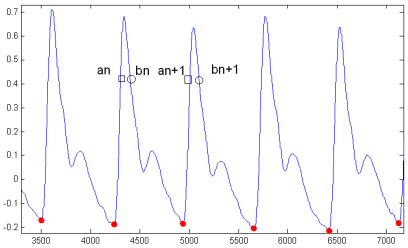

Figure 7. Waveform graph of extraction minimum P4

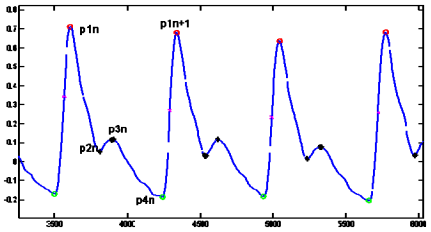

Figure 8. P2, P3 extraction waveform graph

Calculate P2 and P3 methods are as follows:

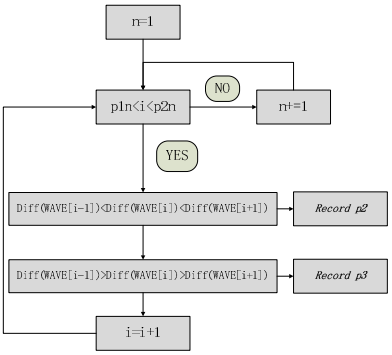

Figure 9. P2, P3 extraction flow chart

The method of looking for P4 is to find the minimum value point from the coordinate at the end of each region, until the beginning of next area coordinates. Each minimum point is all p4 point. See Figure 7.

While the searching method of P2, P3 is searching from the beginning of each P1x axis coordinate until the p4x

coordinates. The point derivatives change from negative to positive is P2. The point derivatives change from positive to negative is P3. See Figure 8.

IV. Pulse Wave Feature Extraction Through FPGA

A. Module overview

This process realizes the four feature point extraction of the given pulse sequences, and displays in the LCD screen. The method is to design a CPU containing PIO by using SOPC technology in Quartus II, and links it with LCD chip. C language feature point is calculated in Nios II software, and display it in LCD screen.

B. LCD display module

The LCD module requires the method use of SOPC and sets up a circuit containing a CPU soft core and a LCD chip in Quartus II software. And add peripheral LCD screen to FPGA chip by using the liquid crystal screen 640 × 480 TFTAA084VC03.

The basic element of LCD screen is TFT tube. TFT (Thin Film Transistor) refers to the thin film transistor. That is each liquid crystal pixel is drived by the thin film transistors at the back of pixel, which can achieve high speed, high brightness, high contrast in displaying screen information. It is one of the best LCD color display devices. Each pixel of TFT is controlled by the TFT integrated on it. It is an active pixel. Therefore, not only the speed can be greatly increased, and the contrast and brightness are greatly improved. At the same time the resolution has reached a very high level. The experiment established TFT_LCD_IP kernel in SOPC Builder, simulated software LCD time series control, wrote program control liquid crystal display in Nois II [8]. Liquid crystal display process is: (1) confirm point position through (X, Y) coordinate; (2) proceed color fill through the sixteen hexadecimal. Single chip LCD's Bdf diagram is as follows: it can be seen that the input signal includes a clock signal, a reset signal, read and write signal, address and data bus; and various output signals, including the color value signal of controlling RGB and output clock signal.

Because SOPC Builder has no bus expansion function, this experiment also uses a custom IP nuclear, expands bus. Specifically extract 8 bits data bus, 3 bits of the address bus, a read signal (active low), write (active low) signal and the strobe signal (low effective lead, direct) of the Avalon bus and connect it with TFT_LCD_IP controller.

After designing LCD connection in Quatus II, pins allocation and compile download can be assigned, and then design drawing function in Nios II. In this program we designed painting point function, drawing line function, square function, filling the square function, drawing circle function, and character display function. It is noted that, in the process of the implementation of characters functions displaying. The cured one or two GB font library is required to be used in the Flash on experimental box. Firstly state clearly read and write basic operation of Chinese characters through simple method, then use the font library in Flash, and display a complete sentence in the program. Each function prototype is as follows:

```
void Draw_Pixel(U16 x， U16 y， alt_u16 color);
//draw point on the position (x，y)
void DrawLine(U16 x1，U16 y1，U16 x2，U16 y2， U16 color);
//segment from(x1，y1)to(x2，y2)
void DrawRect(U16 xp， U16 yp， U16 xl， U16 yl， U16 color);
//draw rectangle
void DrawFillRect(U16 xp， U16 yp， U16 xl， U16 yl， U16 color);
//draw filling rectangle
void DrawEllipse(U16 xp， U16 yp， U16 a， U16 b， U16 color);
//draw oval
void DisplayAnyString(U8 *Str， U16 xp， U16 yp， U16 BK_Color， U16 FT_Color); //display random character string
```

Call these display function in the main function main.c, then random picture or character would be on the LCD screen.

V. Summary and Prospect

This paper realizes the goals including: input the collected pulse wave signal into FPGA processing system; as the actual pulse signals have a series of noise like 50 Hz frequency interference, and ECG distraction, noise deduction should be achieved in FPGA internal need; the signals also need to be simply handled, and achieve feature point extraction. The next signal reduction work, including the high sampling rate reduction of pulse wave signal sequence by using four character points, and restore the digital sequence back to analog signals. The design of pulse wave transmission is based on FPGA and SOPC technology. The anticipated effect has achieved by debugging. After being improved, the whole system will be more perfect and can be put into use. The application of this system has considerable practical significance in production.

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