

A Low Power Fast Locking PLL Frequency Synthesizer with Temperature Compensation

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Abstract—A temperature compensated phase-locked loop (PLL) frequency synthesizer with small locking time is presented. The locking speed is improved by combining the methods of direct frequency presetting and dynamic loop bandwidth. A new technique of temperature compensation combining the static temperature compensation and the dynamic temperature compensation is proposed to effectively reduce the variation of the presetting frequency with the temperature, and high precision frequency presetting and fast locking in a wide temperature range are achieved. The proposed PLL frequency synthesizer is implemented in 180nm CMOS process. The simulation results show that the power consumption is 5mA from 1.8V power supply, and the typical locking time is less than 2 μ s in the temperature range of 0°C~80°C. The output frequency range is 2.1GHz to 2.6GHz, and the phase noise is -117dBc/Hz@1MHz. The designed PLL frequency synthesizer can be widely used in today's communication systems.

Keywords—PLL; fast locking; temperature compensation

I. INTRODUCTION

The PLL frequency synthesizer (PLL for short below), which provides the carrier signal to the radio frequency transceiver is known as the “heart” in wireless communication system. An important parameter in the PLL design is the locking time, which refers to the time that output signal is changed from one frequency to another frequency with the required frequency accuracy.

With the improvement of data rate in the field of communication in recent years, the locking time of the PLL has increasingly become a key parameter in the design of the transceiver circuits. The methods of reducing the locking time are mainly the dynamic loop bandwidth [1] and the direct frequency presetting [2-3]. Since the loop bandwidth is limited by the channel spacing and the spur requirement of the system, the dynamic loop bandwidth method has limited reduction in the locking time. The direct frequency presetting method presets the voltage controlled oscillator (VCO) to the target frequency. Theoretically, if the presetting frequency of the VCO is accurate enough, the PLL can be locked in a very short time, and the locking time does not depend on the frequency hopping amplitude. However, this method has a serious problem at present that the relationship between the presetting signals and the VCO presetting frequencies will change with the temperature, thus the same presetting signals will correspond to different presetting frequencies when the temperature varies, so the direct frequency presetting method

is not so effective as the theoretical prediction. The current method of the temperature compensation in the VCO design still has frequency deviation of several Mega Hz in a wide temperature range [4], and this frequency error is unacceptable for the direct frequency presetting PLL.

Therefore, this paper proposes a fast locking PLL, of which the locking time is reduced by combining the methods of direct frequency presetting and dynamic loop bandwidth. A new temperature compensation technique combining the static temperature compensation and the dynamic temperature compensation is presented to improve the frequency presetting precision and to reduce the locking time in a wide temperature range. The designed PLL can be widely used in today's fourth generation mobile communication systems.

The paper is organized as follows: The second section gives the architecture and the working principle of the PLL, the third section gives the detailed analysis of the PLL circuit, the fourth section gives the simulation results, and the last section is the conclusion.

II. THE PLL ARCHITECTURE AND WORKING PRINCIPLE

Figure I shows the architecture of the PLL circuit which consists of a phase frequency detector (PFD), a charge pump (CP), a second-order loop filter (LPF), a mixed-signal LC VCO, a temperature switch array, a dual mode prescaler (DMP), a digital processor and a nonvolatile memory (NVM).

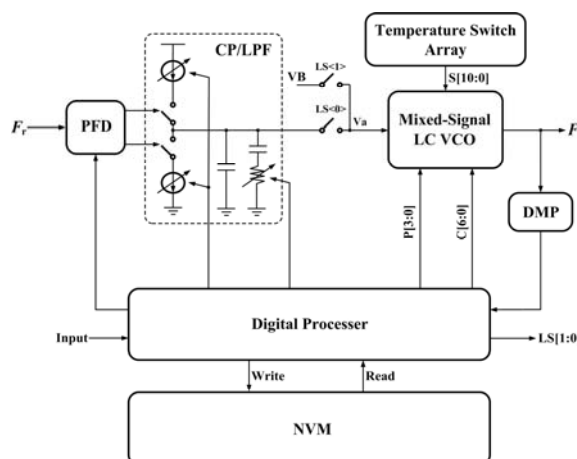


FIGURE I. THE ARCHITECTURE OF THE PLL

The temperature switch array output digital signals $S[10:0]$ to calibrate the relationship between the frequency of the VCO and the temperature, achieving the dynamic temperature compensation, therefore increasing the frequency presetting precision in a wide temperature range.

The PLL operates in the following two modes: calibration mode and operation mode. In the calibration mode, the digital signals $LS[1:0]$ are set to "10" by the digital processor, so the PLL is in open mode and the input of the mixed-signal VCO is biased at a fixed voltage V_B . After that, the digital processor is inputted the frequency information of the hopping target frequency, then the digital processor calculates the digital frequency presetting signals $P[3:0]$ and $C[6:0]$ automatically by interpolation, and the $P[3:0]$ and $C[6:0]$ are then stored in the NVM by the digital processor. In the operation mode, the digital signals $LS[1:0]$ are set to "01" by the digital processor, so the PLL is in working mode. According to the hopping target frequency, the digital processor reads the $P[3:0]$ and $C[6:0]$ corresponding to the target frequency from the NVM, and gives the presetting signals to the mixed-signal VCO to complete the frequency presetting. At the same time, the digital processor controls the CP and the LPF to increase the loop bandwidth of the PLL. The temperature switch array can automatically compensate the temperature variations, and the digital processor can automatically compensate the CMOS process variations [3], so the frequency presetting can achieve very high accuracy and the frequency locking can be completed in a very short time with the locking time not depending on the frequency hopping amplitude.

III. THE CIRCUIT DESIGN OF THE PLL

A. The Mixed-signal VCO Circuit

Figure II shows the circuit of the mixed-signal VCO which consists of a LC VCO and a frequency presetting module. The LC VCO uses the PMOS and NMOS complementary structure to provide a negative resistance, so the conduction current needed to produce the negative resistance can be reduced.

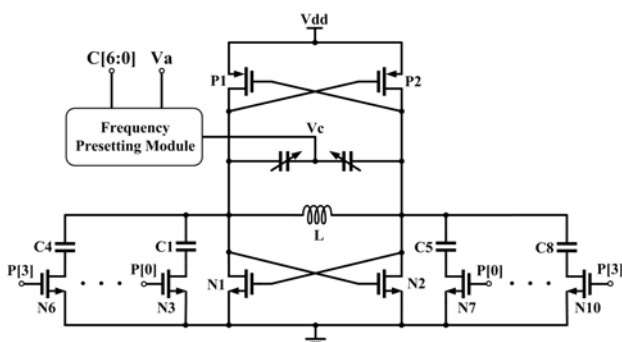


FIGURE II. THE CIRCUIT OF THE MIXED-SIGNAL VCO

The frequency presetting signals $P[3:0]$ control the capacitor array, so 16 tuning curves are created which can cover a wide frequency tuning range. For a certain $P[3:0]$ and a certain voltage V_c , the VCO frequency will change with the temperature. The simulated curve of the VCO frequency versus temperature is shown in Figure III ($P[3:0]=0011$).

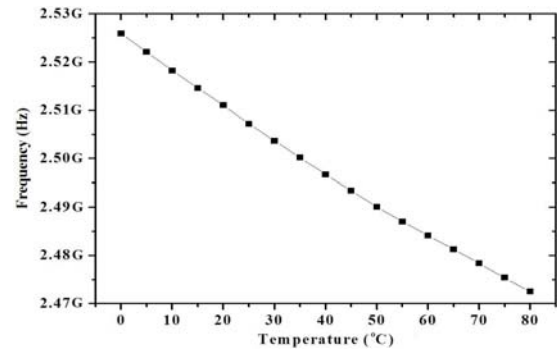


FIGURE III. THE VCO FREQUENCY VERSUS TEMPERATURE

When the temperature is from 0°C to 80°C, the frequency decreases gradually and the frequency variation is more than 50MHz which is an unacceptable value for direct frequency presetting. Therefore, in order to ensure high frequency presetting accuracy in a wide temperature range, the output voltage V_c of the frequency presetting module should increase with the increasing temperature to compensate the tendency of decreasing frequency with the increasing temperature.

The circuit of the frequency presetting module, which consists of a voltage controlled current source (P5), a current source array, a dynamic temperature compensation circuit and a bias circuit is shown in Figure IV.

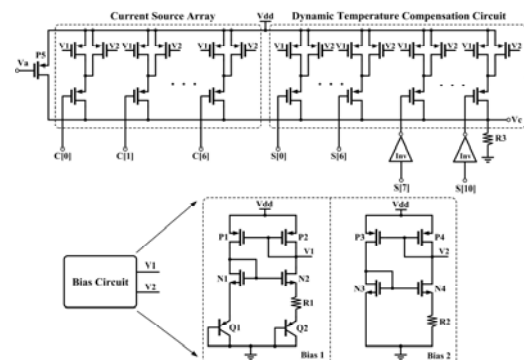


FIGURE IV. THE CIRCUIT OF THE FREQUENCY PRESETTING MODULE

The following analysis first ignores the effects of the dynamic temperature compensation circuit for better understanding the frequency presetting module. The frequency presetting signals $C[6:0]$ control the current source array which consists of binary weighted connection of basic units of two PMOS transistors in parallel. The bias circuit generates two voltages $V1$ and $V2$ to bias the current source array, then the voltage V_c is generated according to the $C[6:0]$, therefore the $C[6:0]$ and the VCO frequency are one by one corresponding. The VCO frequency will change a certain value when changing the $C[6:0]$ of 1 bit. The voltage V_c is set to near 0.9V at which the frequency tuning curves have better linearity and the frequency presetting accuracy is higher.

In order to increase the frequency presetting accuracy in a wide temperature range, the voltage V_c should increase with the increasing temperature. Therefore, the proportional to the absolute temperature (PTAT) current source which is the bias

1 in the bias circuit is used to produce a current proportional to the temperature, and this current is mirrored to the current source array. However, the simulation result shows that the voltage V_c increases rapidly with the increasing temperature, causing the VCO frequency increases rapidly with the increasing temperature, and the frequency varies greatly in a wide temperature range. Therefore, the other type of current source which is the bias 2 in the bias circuit should be combined to compensate the PTAT current source, and this current is also mirrored to the current source array. Now each current source in the current source array is made up of two PMOS transistors in parallel whose gates are connected with the voltages of V1 and V2 from the different current sources in the bias circuit. In this way, the total current of the current source array has a smaller increasing speed with the increasing temperature than that of the PTAT current source, and the producing voltage V_c increases reasonably with the increasing temperature, thus compensating the decreasing of the VCO frequency with the increasing temperature and reducing the change of the VCO frequency with the temperature.

The simulated curve of the VCO frequency versus temperature is shown in Figure V under the conditions of $V_a=V_b$, $P[3:0]=0011$ and $C[6:0]=1100000$.

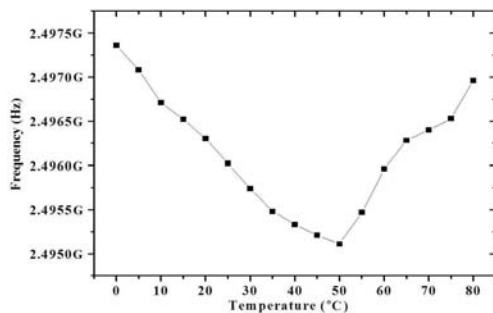


FIGURE V. VCO FREQUENCY VERSUS TEMPERATURE

As shown in Figure V, in the range of 0°C to 80°C, the VCO frequency has a small change less than 2.5MHz. The VCO frequency first decreases with the increasing temperature and then increases with the increasing temperature. Although the frequency presetting module reduces the change of the VCO frequency to less than 2.5MHz, this frequency error is still larger for the direct frequency presetting. Since the VCO frequency and temperature are essentially nonlinear relationship, it is difficult to further reduce the change of the VCO frequency using static temperature compensation technique in a wide temperature range.

Although the VCO frequency varies greatly in a wide temperature range, the frequency change is small in a small section of the temperature, e.g., if the section of the temperature is selected as 5°C, the frequency change will be less than 0.5MHz. Therefore, if the voltage V_c is revised every a certain interval of the temperature, the frequency change in a wide temperature range will be reduced to the frequency change in a small section of the temperature. To this end, the dynamic temperature compensation circuit, which consists of 11 current sources is added to the frequency presetting module. The 11 bit digital signals $S[10:0]$ from the temperature switch array control the 11 current sources. The temperature switch is

such a circuit that changes its output voltage abruptly from high level to low level when the temperature increases to a certain threshold temperature. The temperature switch array consists of 11 temperature switches with different threshold temperature. When the temperature changes from one section to the next section, the state of the $S[10:0]$ changes, turning on or turning off the corresponding current source in the dynamic temperature compensation circuit, so that the V_c is hopped and the VCO frequency raises or drops to the initial value in the previous section of the temperature.

Considering the dynamic temperature compensation circuit, the simulated curve of VCO frequency versus temperature is shown in Figure VI. The temperature range of 0°C to 80°C is divided into 13 temperature sections, and the maximum frequency change is less than 0.5MHz in each temperature section. The average frequency error is less than 0.3MHz which is about one order of magnitude smaller than that of the non dynamic compensated VCO, and is an acceptable value for the direct frequency presetting.

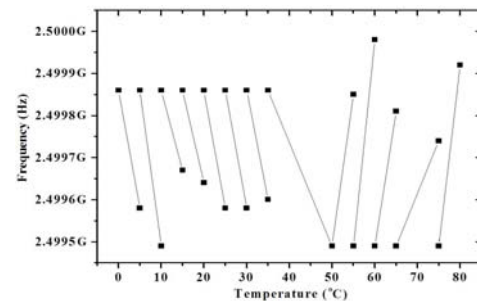


FIGURE VI. VCO FREQUENCY VERSUS TEMPERATURE AFTER THE DYNAMIC TEMPERATURE COMPENSATION

B. The Circuit of the Temperature Switch Array

Figure VII shows the temperature switch array which consists of 11 temperature switches with different threshold temperature. Each temperature switch has the same circuit structure. When the temperature exceeds the threshold temperature of a certain temperature switch, the output digital signal $S[k]$ ($k=0\sim10$) of the temperature switch will change from high level to low level, changing the state of the output signals $S[10:0]$ of the temperature switch array.

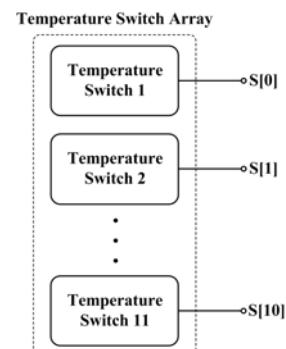


FIGURE VII. THE CIRCUIT OF THE TEMPERATURE SWITCH ARRAY

The circuit architecture of the temperature switch is shown in Figure VIII.

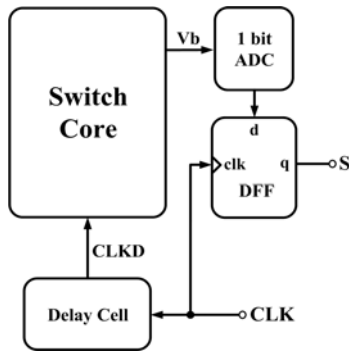


FIGURE VIII. THE CIRCUIT ARCHITECTURE OF THE TEMPERATURE SWITCH

The temperature switch consists of a switch core, a 1 bit ADC, a D flip-flop (DFF) and a delay cell. The switch core, which is the core module in the temperature switch is used to perform the temperature switch function in analog domain. The 1 bit ADC is used to convert the analog voltage V_b to the digital signal which is sampled by the following DFF to output the digital signal S. The delay cell, which consists of several inverters in series guarantees that the clock timing is working properly.

The circuit of the switch core, which consists of a key switch circuit and a compensation circuit is shown in Figure IX [5]. The different threshold temperature can be obtained by adjusting the parameter $K_{43}=(W/L)_4/(W/L)_3$, where the W and L are the channel width and length of the corresponding NMOS transistor respectively. The voltage V_b changes abruptly from high voltage to low voltage of nearly zero when the temperature exceeds the threshold temperature of the temperature switch. The range of the threshold temperature of the temperature switch array is from 5°C to 75°C.

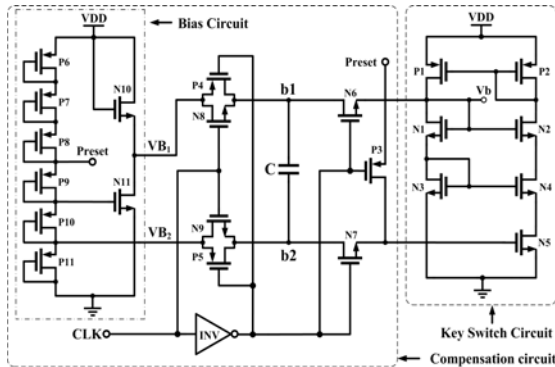


FIGURE IX. THE CIRCUIT OF THE SWITCH CORE

IV. SIMULATION RESULTS

The designed fast locking PLL frequency synthesizer is implemented and simulated in 180nm CMOS process. Figure X gives the relationship between the VCO frequencies and the frequency presetting signals P[3:0] and C [6:0] in the case of $V_a=0.9V$. The simulation result shows that there is a good linear relationship between the presetting frequencies and the frequency presetting signals under three sets of the P[3:0].

Considering there will be 16 sets of the P[3:0] signals actually, the frequency range of the PLL is from 2.1GHz to 2.6GHz.

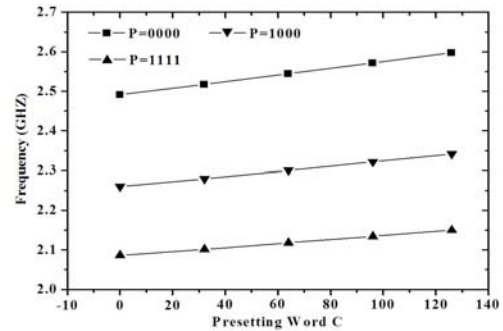


FIGURE X. THE RELATIONSHIP BETWEEN THE VCO FREQUENCIES AND THE FREQUENCY PRESETTING SIGNALS

After the calibration mode is completed at 27°C, the frequency hopping is performed every 5°C interval in the range of 0°C to 80°C, and the obtained typical locking time is less than 2μs. Figure XI gives the frequency hopping characteristics of the PLL at 60°C.

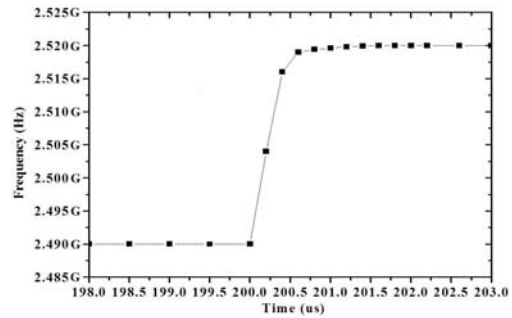


FIGURE XI. THE FREQUENCY HOPPING CHARACTERISTICS OF THE PLL

The frequency of the PLL is rapidly hopped from 2.490GHz to 2.520GHz at 200μs, and the locking time is less than 2μs. The summary of the performance parameters of the PLL is shown in Table I.

TABLE I. SUMMARY OF THE PERFORMANCE PARAMETERS OF THE PLL

Parameters	Simulation results
Process	180nm CMOS
Voltage supply	1.8V
Current consumption	5mA
Frequency range	2.1GHz~2.6GHz
Phase noise	-117dBc/Hz@1MHz
Typical locking time	<2μs (0°C~80°C)
Loop bandwidth	0.2MHz~2MHz
Frequency presetting accuracy	<0.5MHz (0°C~80°C)

V. CONCLUSION

A PLL frequency synthesizer combining the methods of direct frequency presetting and dynamic loop bandwidth is presented to accelerate the locking speed of the PLL. A new temperature compensation technique is proposed which greatly improves the frequency presetting accuracy in a wide temperature range. The simulation results show that the frequency presetting accuracy is less than 0.5MHz, and the typical locking time is less than 2 μ s in the temperature range of 0°C to 80°C. The phase noise is -117dBc/Hz@1MHz in the case of the power consumption of 5mA from 1.8V power supply. The designed PLL has the characteristics of high locking speed in a wide temperature range. It can be widely used in today's communication systems.

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