A High Speed Amplifier Used in High-resolution GSPS Pipelined ADC

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Abstract. In this paper, a high speed amplifier used in high-resolution GSPS pipelined ADC is described. To satisfy a 14bit 1GSPS ADC accuracy and speed demand, The high speed amplifier adopts two-stage Miller compensation architecture. To increase amplifier gain, active gain-boosted cascodes and cross-coupling positive feedback are used in the first stage of the amplifier. To improve phase margin and settling of the amplifier, big resistor and inductor are used in the second stage of the amplifier. The high speed amplifier used in a 14bit 1GSPS pipelined ADC fabricated on a 65nm CMOS process achieves a closed loop gain of 82dB, a closed bandwidth of 4.0GHz, phase margin of 70 degree, dissipates 250mW power, occupys 0.11mm^2 area.

Introduction

Today, many applications including wireless communication,software defined radios,radar syetem etc demand high-resolution A/D converters(ADCs) with high sample rate,good AC performance and RF sampling capability. Generally, higher sample rates ADC has larger bandwidth,can simplify system and anti-aliasing filters design, lower the system cost and improve the overall system performance and efficiency.

Pipelined ADC is the main architecture of High speed and high-resolution ADC. Pipelined ADC can achieve relatively high resolution and good linearity throughout the whole Nyquist bandwidth.

It is known that Pipelined ADC consists of several pipeline stages. Each stage of the pipeline ADC, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier(RA) magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The performance of residue amplifier decides directly the performance of the whole Pipelined ADC, such as speed and precision. In this paper, a high speed low power residue amplifier used in 14 bit 1GSPS Pipelined ADC is described.

Section 2 gives a overview of the Pipelined ADC architecture. Section 3 gives a detailed circuit description of the high speed residue amplifier. Section 4 gives simulation results and layout design of the residue amplifier. Section 5 is conclusion.

A 14bit 1GSPS Pipelined ADC Architecture Overview

A block diagram of the 14-bit ADC architecture is shown in Fig.1. This SHA-less ADC consists of a differential input buffer followed by six pipeline stages. The differential input buffer accepts a 2Vp-p differential signal. Following the input buffer is a 3-bit MDAC with 1 bit of redundancy to improve comparator offset tolerance. The 3-bit MDAC is followed by another four 3-bit MDAC with 1 bit of redundancy. The final 4 lsb's are converted by the backend 4 bit flash converter.

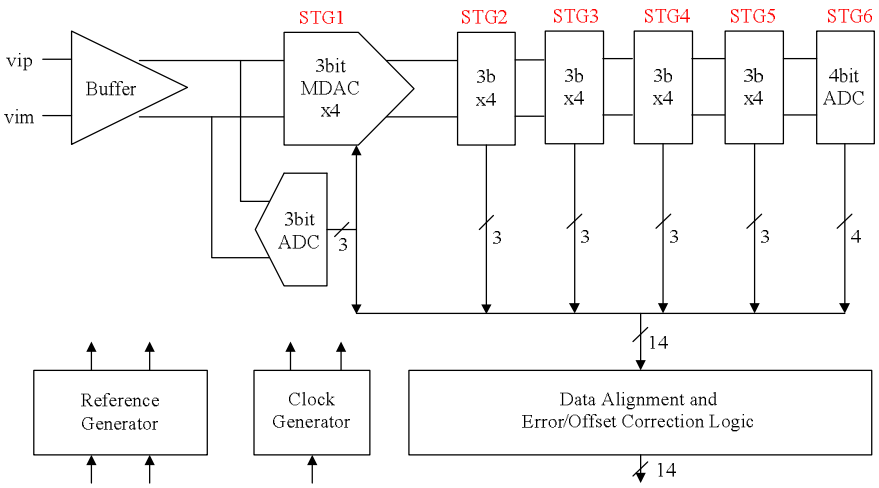

Fig. 1 14-bit ADC architecture

Each stage of the pipeline consists of sub ADC、DAC and residue amplifier. The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

This ADC also includes reference and clock generator. A differential voltage reference creates positive and negative reference voltages that define the 2Vp-p fixed span of the ADC core. A clock circuit based on dynamic delay line (DLL) provides all kinds of phases clock to every part of the pipelined ADC.

High Speed Residue Amplifier Circuit

This ADC have a SHA-less analog front end. Followed the low distortion input buffer, a 3bit architecture is chosen for the ADC's 1st stage. One bit redundancy is added to increase the sub-ADC comparator offset tolerance. Multi-bit/stage architecture has been widely used in high speed and high resolution pipelined ADC designs, especially in ADC's front end stages. It has the advantage of reducing the capacitor matching requirement, improve ADC linearity. Fig.2 shows the 1st stage pipeline architecture.

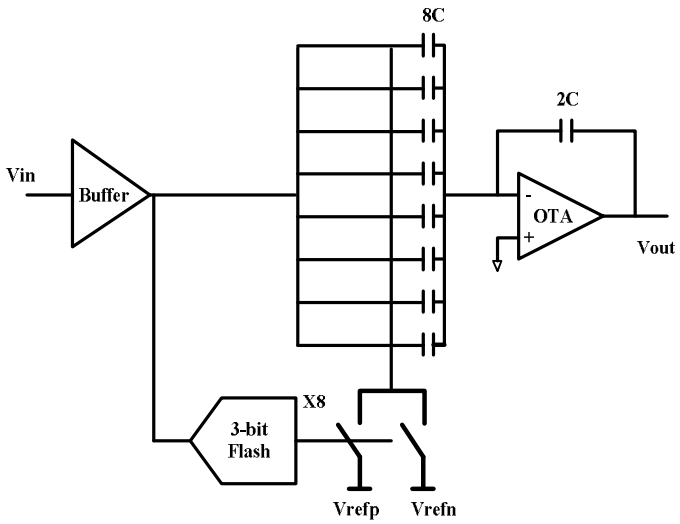

Fig.2 1st stage pipeline architecture

The 1st stage flash ADC has sampling networks for its comparators that closely match that of the MDAC. This is needed because any mismatch in the comparators causes the input value sampled by the MDAC to be different from that sampled by the comparators. This leads to flash offset and gain errors that get worse with increasing the input frequency. This error consumes a portion of the correction range of the first stage residue and can be corrected by the digital error correction only as long as the

residue does not exceed the correction range. During the sampling phase, the input is sampled on the MDAC and the flash sampling capacitances. During the hold phase, the flash comparators make their decisions and propagate them to the DAC switches, which connect the DAC capacitances to either Vrefp or Vrefn depending on the flash bits. Fig.3 shows the 1st stage output residue curve.

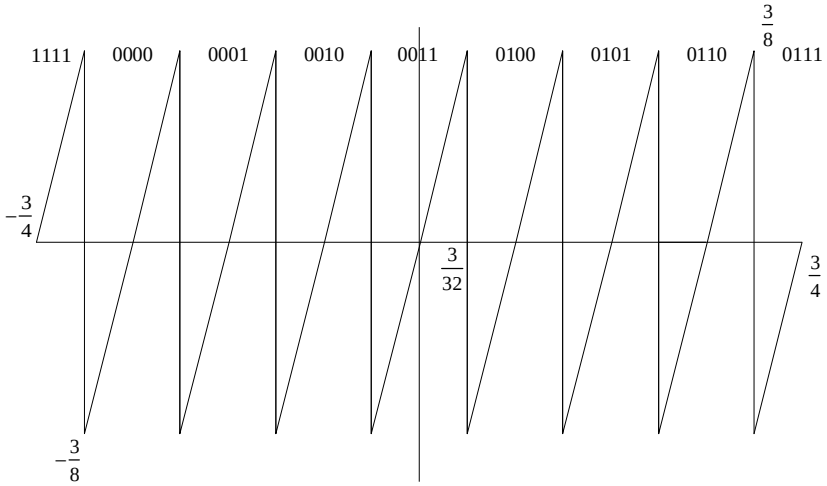

Fig.3 1st stage output residue curve

The high speed residue amplifier, shown in Fig.4, is a two stage Miller compensated amplifier with active gain-boosted cascodes in the first stage and a differential pair in the second stage. The input stage adopt NMOS transistors and PMOS loads. The NMOS differential input transistors connect to NMOS cascodes, then output to the second stage. Similarly, the PMOS loads connect to PMOS cascodes. The NMOS and PMOS cascodes have own gain-boosted amplifier, which can improve the whole amplifier gain. Furthermore, the first stage uses positive feedback, through cross-coupling, to create a negative trans-conductance circuit in parallel with the main devices, which can improve the gain more. The first stage have also a tail current source controlled by common mode feedback (CMFB1)block.

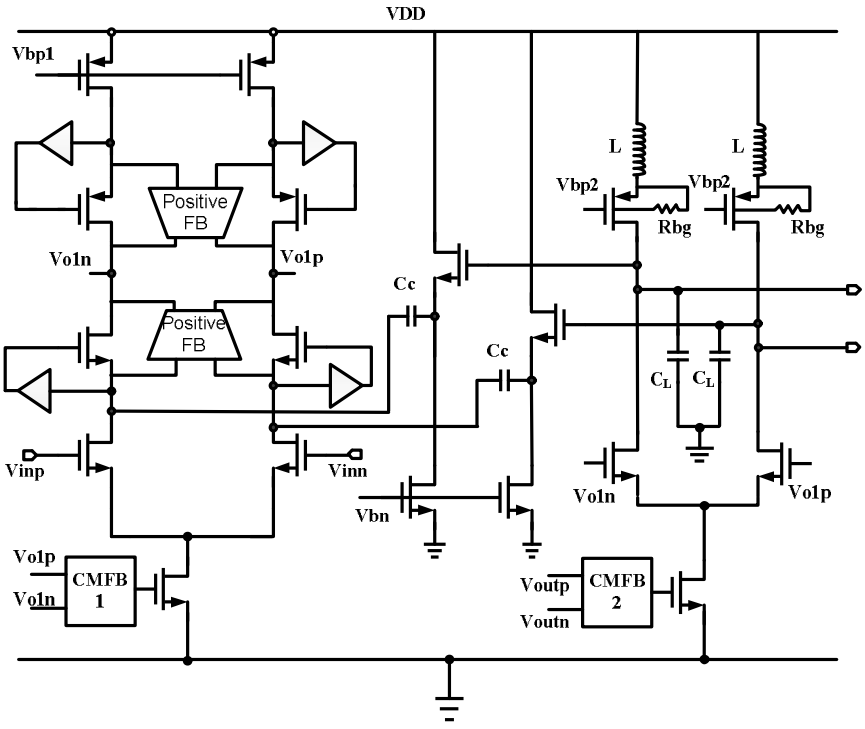

Fig.4 novel high speed residue amplifier architecture

The back-gates of the second stage's PMOS transistor is not connect to VDD supply directly, but via a big resistor to VDD supply. This cause original main drain capacitance(Cdb) to be in series with the n-well capacitances of the PMOS transistor, hence decrease the whole parasitic capacitance of output node. Furthermore, the source of PMOS connect to VDD supply via a an on-chip inductor. The

inductor L, the resistor Rbg and the load capacitance C_L form an RLC circuit that has a pair of complex poles.

The small signal simple circuit of the impedance of output node, shown in Fig.5, is a RLC parallel connection circuit. The impedance of output node Zout(s) is given by Eq. 1

$$Z\text{out}(s) = \frac{R_N(R_P + Ls)}{LC_L R_N s^2 + (R_N R_P C_L + L)s + R_N + R_P} \tag{1}$$

Where R_N is the output impedance of NMOS transistor, R_P is the output impedance of PMOS transistor, L is the inductor, C_L is the load capacitance.

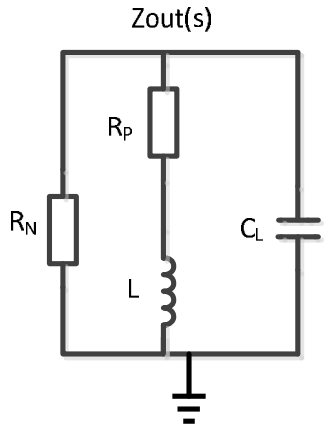

Fig.5 output node impedance's small signal circuit

Inserting the inductor result in adding a zero and a pole to output node. Optimizing inductance can improve the phase margin and settling of the amplifier across supply, temperature and process, compared to a traditional RC load circuit. Using this inductor also lowered the power consumption of the amplifier by about 30% compared to RC load designs.

The second stage have also a tail current source controlled by common mode feedback(CMFB2) block. The Miller compensation capacitances are connected between the outputs of source follower of the second stage and the source of PMOS cascode transistors of the first stage.

Simulation Results and Layout Design

At 1GSPS sample rate, the closed loop bandwidth required for the 1st stage pipeline residue amplifier to achieve 14-bit performance is about 3.8GHz and the closed loop gain needs to be larger than 80dB. This required high gain-bandwidth product leads to high power consumption in 1st stage pipeline.

The high speed residue amplifier performance is summaried in the following table.

Table 1 This high speed residue amplifier performance summary

Technology	65nm CMOS
Supply Voltage	2.5V
Differential Input Range	1.7Vp-p
Closed loop gain	82dB
Closed loop bandwidth	4.0GHz
Phase Margin	70degree
Power Dissipation	250mW

The 14bit ADC is fabricated on a 65nm CMOS process. Fig.6 shows the layout of the high speed residue amplifier. The layout size is 0.32mm X 0.35mm.

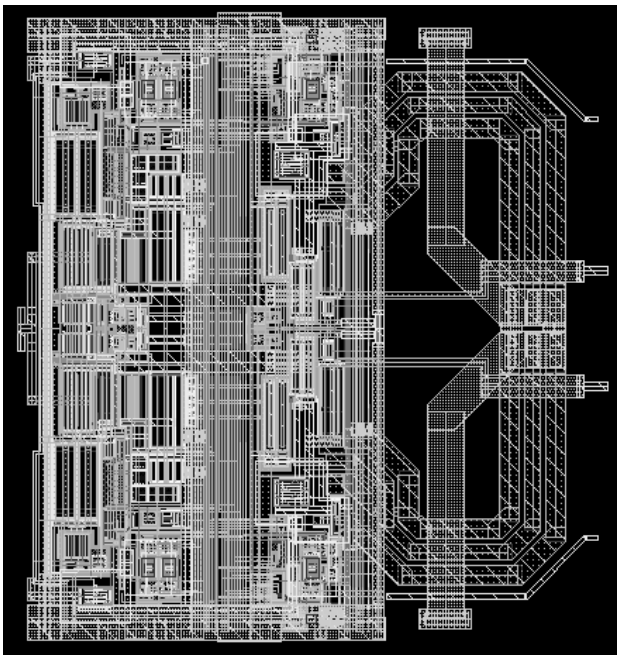

Fig.6 the high speed residue amplifier layout

Conclusion

This paper describes a high speed amplifier used in a 14bit 1GSPS pipelined ADC, introduces 14bit 1GSPS pipelined ADC's architecture and high speed amplifier circuit design. The high speed amplifier fabricated on a 65nm CMOS process achieves a closed loop gain of 82dB, a closed bandwidth of 4.0GHz, phase margin of 70 degree, dissipates 250mW power, occupys 0.11mm^2 area.

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