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Design and Implementation of a Required-Input Multi-Signal Generator

Baotang Shan*, Bo Chen and Xiaohang Ren
Department of Communication and Tracking, Changping NCO School of Space Engineering University, Beijing 102249, China
*Corresponding author

***Abstract*—To meet the special need of test, experiment, training and teaching, a design scheme of a required-input multi-signal generator is presented. FPGA and DSP are used to generate baseband signals, including HDB3 code, Manchester code, CMI code, Miller code, and frequency band signals, including ASK, FSK and PSK. With imitated-original data stimulating, simulations are completed and part simulation results are shown. Based on hardware test bed, application tests are finished and part test results are given. It is proved that the scheme is valid and practical.**

Keywords—signal generator; fpga; dsp; simulation

I. INTRODUCTION

The required-input multiple signal generator follows the input data of experiment task to generate baseband signals and frequency band signals. To meet the requirements of testing, analyzing, teaching and training, the baseband signals include High Density Bipolar of Order 3 (HDB3) code[1], Manchester code, Miller code, Code Mark Inversion (CMI) code, Not Return to Zero (NRZ) code and the frequency band signals[2] include Binary Amplitude Shift Keying (2ASK) signal, Binary Frequency Shift Keying (2FSK) signal, Binary Phase Shift Keying (2PSK) signal, Quarter Phase Shift Keying (QPSK) signal, Eight Phase Shift Keying (8PSK) signal, pure carrier signal and so on.

II. OUR DESIGN

FPGA[3,4]+DSP[5] scheme is employed in our system design, which is illustrated as Figure I.

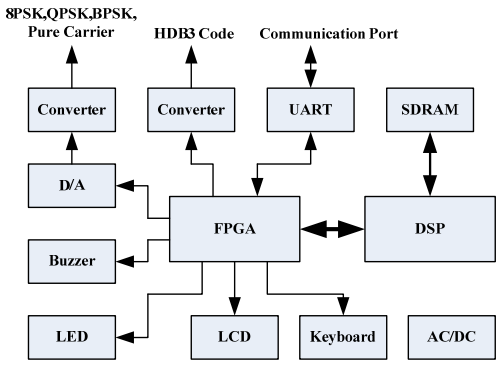


FIGURE I. OUR DESIGN SCHEME

In the design, DSP is used as processing core and FPGA is used as extending ports, which include keyboard module, buzzer, LCD displaying module, LED and etc. More importantly, FPGA is used to generate multiple signals, including HDB3, CMI, Manchester, ASK, FSK, PSK and etc. Keyboard and keyboard module are used to input digital information following requirement. A buzzer is designed in the system to give out tip voice when necessary. LCD and LCD displaying module are used to display useful information, which is completed in DSP. LED lights give some necessary indications to show system states. UART is a serial communication port, which is very useful when the system is connected to a computer or administrated remotely. AC/DC module converts 220V alternating current to +5V direct current, which is used in our system design. Last but not least, an 8-bit digital to analog convertor is applied to smooth frequency signals, which makes sure that the quality of the output signals is good.

The FPGA design of baseband signal generator is illustrated as Figure II, where Converter8To1 module is a convertor of 8-bit parallel data to serial data. In the figure, HDB3 code is generated by add_V, add_B and Alter module, and Miller code by MillerCode module, CMI code by CMICode module. The function of add_V module is to insert V code in serial data and add_B is to insert B code. Alter module is to alternate polarity of the output serial data, where the principle is that V code is alterative following itself and the polarity of B code or information code is the same as the polarity of the V code just before it. There is no negative voltage in FPGA, so encoding of output voltage is needed, where 50 percent empty is converted before output. In our system, a data selector is used as HDB3 code generator, which has two data input ports and two address input ports. One data input port is connected to +5V voltage and the other is connected to -5V voltage. Two address input ports, which are connected to encoding module in FPGA, uses encoding level of HDB3 as address of the data selector to complete dual-polarity output.

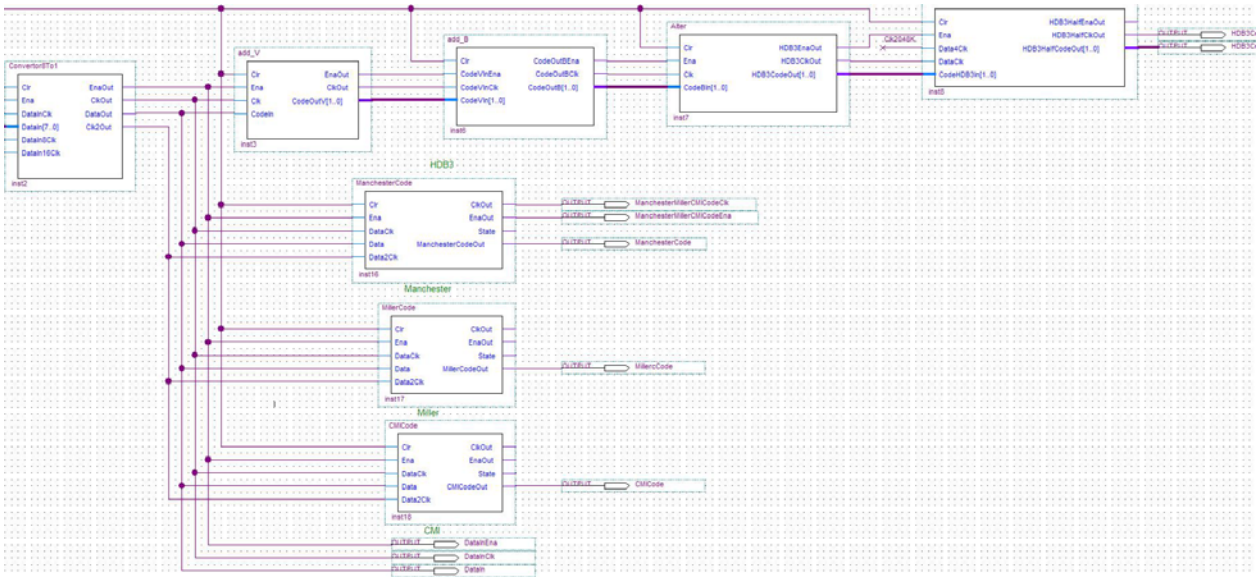


FIGURE II. FPGA DESIGN OF BASEBAND SIGNAL GENERATOR

Simulation of HDB3 coding generation is shown in Figure III, where the test data are 0,1,2,3,4,……, 255 and the data clock is Clk2048K. Clr is an asynchronous clear signal which is active when high. Clk12M is 12MHz system clock. Clk896K, Clk2048K and Clk8192K are three output clocks of phase locked loop (PLL) in FPGA. The part of high-impedance is steady course of PLL, and Locked means the PLL has been locked and steady when the system can work properly. HDB3ClkOut is a data clock and HDB3CodeOut are the data coded of HDB3, where "01"means positive voltage and "11"means negative voltage. HDB3EnaOut is an enable signal of HDB3. HDB3HalfClkOut, HDB3HalfCodeOut, HDB3HalfEnaOut are data clock, data coded and enable signal, which are 50 percent empty.

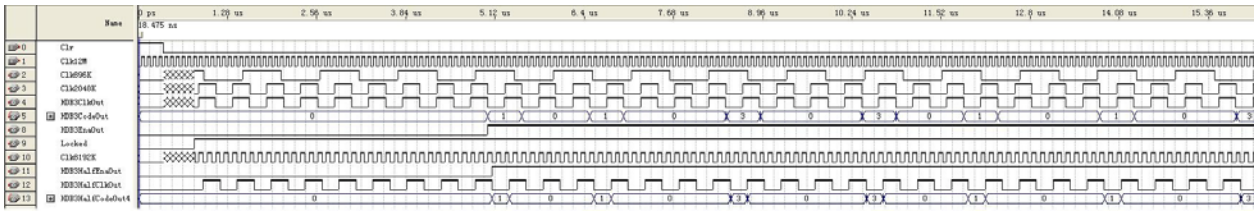


FIGURE III. PART SIMULATION RESULTS OF HDB3 CODE

ManchesterCode module, MillerCode module, CMICode module generate Manchester code, Miller code and CMI code respectively, following serial data input. Part simulations are illustrated as Figure IV, Figure V and Figure VI.

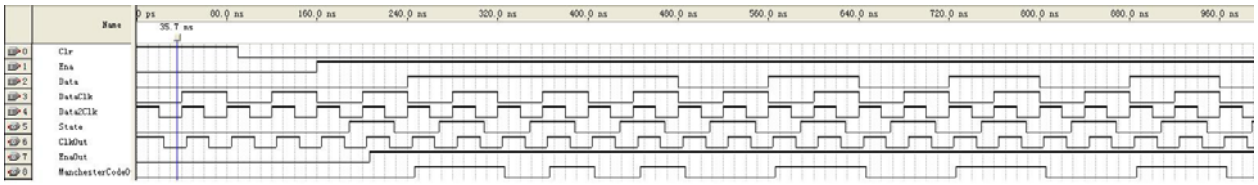


FIGURE IV. PART SIMULATION RESULTS OF MANCHESTER CODE

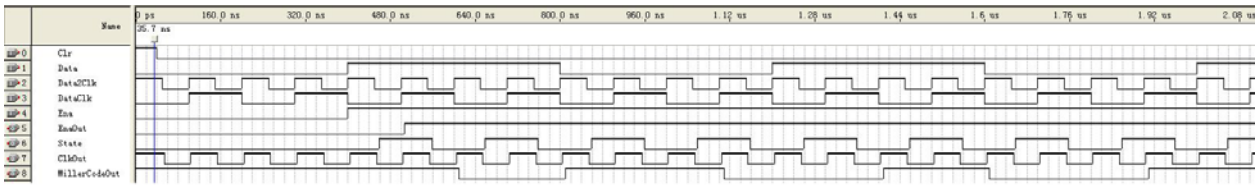


FIGURE V. PART SIMULATION RESULTS OF MILLER CODE

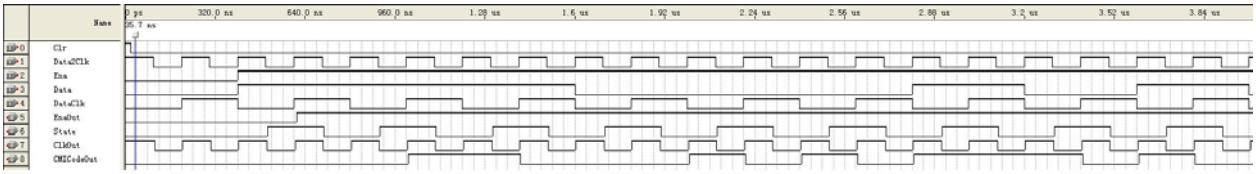


FIGURE VI. PART SIMULATION RESULTS OF CMI CODE

The FPGA design of the generator of frequency band signals is illustrated as Figure VII, where ModSti generates pure carrier, ASK, FSK and PSK data. ASK_FSK_PSK_Sel module is a multi-function data selector, which selects signal input following Mode_Sel. Clk128K, Clk512K are clock with 128KHz and clock with 512KHz clock. Mode_sel[3..0] are inputs of working mode, which have 16 address ports from “0000”to “1111”. DataIn[7..0] are data of 8 bits per symbol that are input from DSP. There are two ModSti modules are used to generate FSK signal. In fact, the function of the second ModSti module is the same as that of the first, where the first module uses Clk128K, which is the clock of 128KHz, and the second uses Clk512K, the clock of 512KHz.Part sampled data of cosine curve are given in Figure 8, which are 128 points per cycle and 8 bits per point.

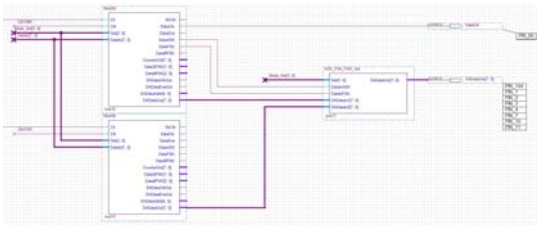


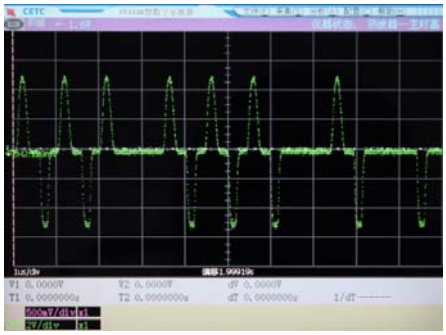
FIGURE VII. FPGA DESIGN OF THE GENERATOR OF FREQUENCY BAND SIGNALS

Addr	+0	+1	+2	+3	+4	+5	+6	+7
0	127	133	139	145	151	158	164	170
8	175	181	187	192	198	203	208	212
16	217	221	225	229	233	236	239	242
24	244	246	248	250	251	252	253	253
32	253	253	253	252	251	249	247	245
40	243	240	238	234	231	227	223	219
48	215	210	205	200	195	190	184	178
56	173	167	161	155	148	142	136	130
64	123	117	111	105	98	92	86	80
72	75	69	63	58	53	48	43	38
80	34	30	26	22	19	15	13	10
88	8	6	4	2	1	0	0	0
96	0	0	1	2	3	5	7	9
104	11	14	17	20	24	28	32	36
112	41	45	50	55	61	66	72	78
120	83	89	95	102	108	114	120	126

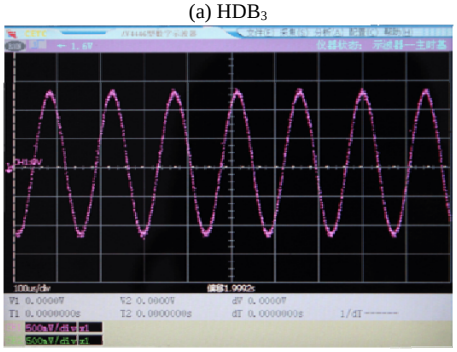
FIGURE VIII. DATA OF 128 POINTS

III. APPLICATION TESTS

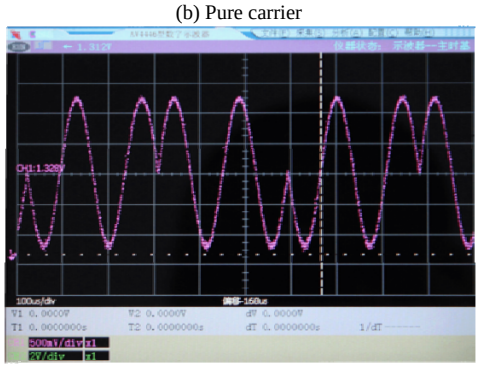
Part test results are given as followed in Figure 9, including HDB3 code, pure carrier, BPSK and QPSK, where 12MHz system clock is used. In the test, the data rate of HDB3 code is 2048 Kbits per second, which is bi-polarity and 50% empty. Pure carrier, BPSK and QPSK are given after digital to analog conversion, where two cycles represent one symbol. In Figure 9(c), 0 phase position means “0”and Pi means “1”. In Figure 9(d), 0 phase position means “00”, Pi/2 means “01”, Pi means “10”and 3Pi/2 means “11”.



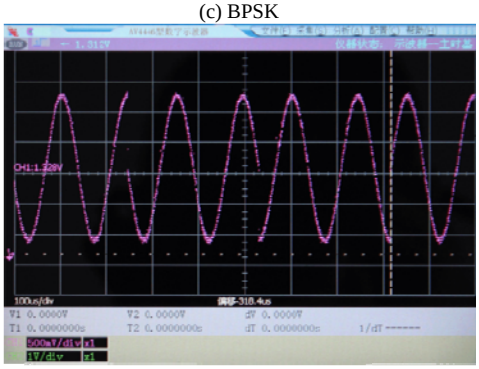
(a) HDB_3



(b) Pure carrier



(c) BPSK



(d) QPSK

FIGURE IX. PART TYPICAL SIGNALS, (A) HDB3, (B) PURE CARRIER, (C) BPSK, (D) QPSK

IV. CONCLUSIONS

Based on requirements of practical application, a design scheme of a multi-signal generator with band signals and frequency band signals is given, which is implemented in FPGA and DSP on hardware platform. Part key techniques in the system are elaborated and part simulation results are illustrated. Finally, part test logic-analyzed results are shown, which demonstrates our scheme is right and feasible.

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