ATLANTIS PRESS
Advances in Engineering Research, volume 149
2nd International Conference on Mechanical, Electronic, Control and Automation Engineering (MECAE 2018)

Design of a High-Performance Ultra-Wideband Monocycle Pulse Generator

Qi Yin [a], Zhongming Pan [b] and Zhuohang Zhang [c]
School of Intellimation, National University of Defense, Changsha 410073, China
[a]yinqisquare760@163.com, [b]chungmingpan@nudt.edu.cn, [c]zhangzhuohang23@163.com

Keywords: Ultra-wideband, Pulse generator, Avalanche transistor, Step recovery diode.

Abstract. A high-performance ultra-wideband (UWB) monocycle pulse generator is described in this paper. The pulse generator circuit is mainly composed of avalanche transistor, step recovery diode (SRD), Schottky diode (SD) and microstrip lines. The proposed circuit solution utilizes the avalanche effect of avalanche transistor to produce driver pulses with high amplitude and sharp edges, which can drive the SRD included in a universal microstrip pulse forming circuit effectively to produce high-amplitude Gaussian pulses. Monocycle pulses are then generated by an additional pulse forming network. The circuit, simulated in the radiofrequency software ADS, can generate monocycle pulse whose pulse full width is 600ps, pulse amplitude is 6.3V peak-to-peak and pulse repetition rate is 10MHz with a ringing level of -24dB and good symmetry. With the features such as high pulse amplitude and stable performance this pulse generator is applicable to UWB system.

1. Introduction

UWB technology has been widely used in the fields of wireless communication [1], ground penetrating radar [2] and see-through-wall imaging [3, 4], owing to its advantages of high rate, low power consumption and low cost. The technique of generating narrow pulse is one of the principal parts of UWB technology and has received many considerations in recent years. At present, there are mainly two methods to generate UWB narrow pulse. One method is using the competition phenomenon of CMOS logic gate circuit [5, 6]. The pulse generated in this way whose pulse width ranges from hundreds of picoseconds to several nanoseconds. However, the pulse amplitude is so small, usually hundreds of millivolts, moreover, the circuit is quite complicated and the state power consumption is relatively high. The other method is using the nonlinearity switch characteristic of semiconductor. In this way, the circuit is simple and easy for realization and integration. The semiconductor components which have high speed switch characteristic mainly incorporate avalanche transistors, tunnel diodes, FETs, SRD and photon conductive semiconductor switches. Among them, avalanche transistors and SRD have been widely used because of their relatively high-performance and low cost. Pulse generators based on avalanche transistors [1, 7-8] utilize the avalanche effect to produce Gaussian pulse whose pulse amplitude is tens of volts, but the pulse width is a bit large. Whereas pulse generators based on SRD [2, 9-10] utilize the high speed transient effect of SRD to produce step pulse, the circuits usually employ pulse shaping circuit and pulse forming circuit to reduce the distortion and invert the step pulse to Gaussian pulse or monocycle pulse. The generated pulse whose pulse width is hundreds of picoseconds, but the pulse amplitude is a bit small.

This paper presents a high-performance pulse generator composed of driver module and pulser module shown in Fig.1. The driver module incorporates a differentiator circuit and an avalanche circuit, the trigger signal can be inverted to a driver pulse with high amplitude and sharper edges by the driver module. Accordingly, the pulser module incorporates a SRD pulse shaping circuit and a monocycle pulse forming circuit, the driver pulse generated by the driver module can be inverted to a monocycle pulse with low ringing level and good symmetry through the pulser module. The innovation of this paper is to synthetically utilize the characteristic of avalanche transistor and SRD, meanwhile combine them well in one circuit. The result is that the monocycle pulse width is greatly

narrowed and the pulse amplitude is kept at a high level. The proposed design is clear and the circuit is simple, so it is suitable to be used as the pulse generator in the UWB system.

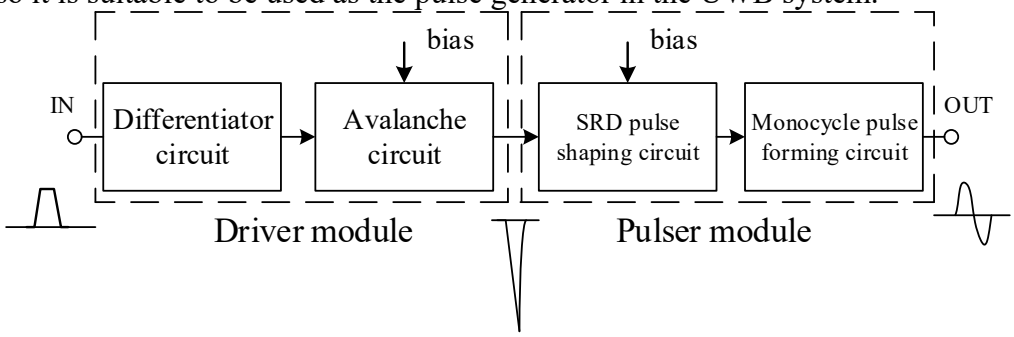


Fig. 1 Block diagram of the UWB pulse generator

2. Circuit Description and Design

2.1 Driver Module.

A circuit diagram of driver module is shown in Fig.2. The driver module adopts double transistors parallel circuit structure. In this way, the output current is superimposed on the load RL, which can effectively increase the amplitude of the output pulse, meanwhile it can shunt the base current which becomes oversized may cause the damage of the transistors. The two parallel branches are exactly the same, the following makes a specific analysis about the topic branch.

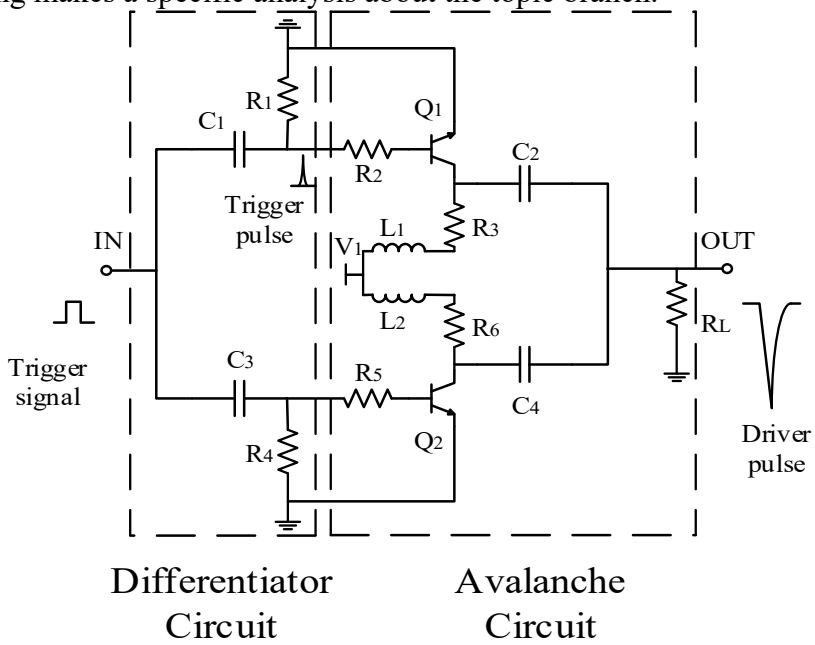


Fig. 2 Circuit diagram of driver module

(a) Differentiator circuit

As shown in Fig.2, the differentiator circuit is composed of R1 (100Ω) and C1 (20pF), its function is to extract the edge of the square trigger signal and reduce the duty ratio for triggering the avalanche circuit well. In one cycle of the trigger signal, the differential capacitance will be charged and discharged each time, so we need insure that $(3\sim5)\tau<T/2$, where $\tau=R1C1$ is the time constant of the differentiator circuit and T is the cycle of the square trigger signal . Besides, from the perspective of amplitude [1], the amplitude of the trigger pulse depends on the values of R1 and C1. The bigger the multiplication of R1 and C1 is, the bigger the amplitude is. Accordingly, the base current of Q1 will be larger which can impel the amplitude of the driver pulse to increase. The two perspectives mentioned above are contradict with each other, so when selecting the values of R1 and C1, we should consider the amplitude and the time constant simultaneously.

(b) Avalanche circuit

The avalanche circuit is composed of R2, R3, L1, C2 and Q1. The DC power V1 (12V) is used to supply the bias voltage to make the transistor Q1 in a critical avalanche state. As described in paper [1], V1 should be less than BVCBO and more than BVCEO of Q1. Respectively, R2 (30Ω) and R3 (680Ω) are the base and collector limit current resistance. C2 (20pF) is a storage capacitor. When there is no trigger signal, Q1 is in cutoff state. Meanwhile, VCC recharges C2 via L1 (10uH) and R3. Notably, L1 plays an important role in the charging process [11], in the one hand, L1 can accelerate the charging process and it is useful to increase the pulse repetition rate. In the other hand, L1 can enhance the voltage of C2 and it is favorable to increase the amplitude of the driver pulse. Whereas when there is a trigger signal, Q1 turns into conduction state rapidly. Meanwhile, C2 discharges to RL (50Ω) via Q1, the avalanche current can achieve at a high level in a cutty time during the discharging process, hence, we can obtain a driver pulse with high amplitude and sharp edges at the output terminal.

2.2 Pulser Module.

A circuit diagram of pulser module is shown in Fig.3. SRD is the core of the pulser module and it has intense nonlinearity. So it's the principal work to establish the SRD model in the software which can represent the nonlinear character of SRD accurately in order to design the pulser module. This paper adopts the method described in paper [12] to realize the SRD model in the software ADS and the model can represent SRD well in the simulation test.

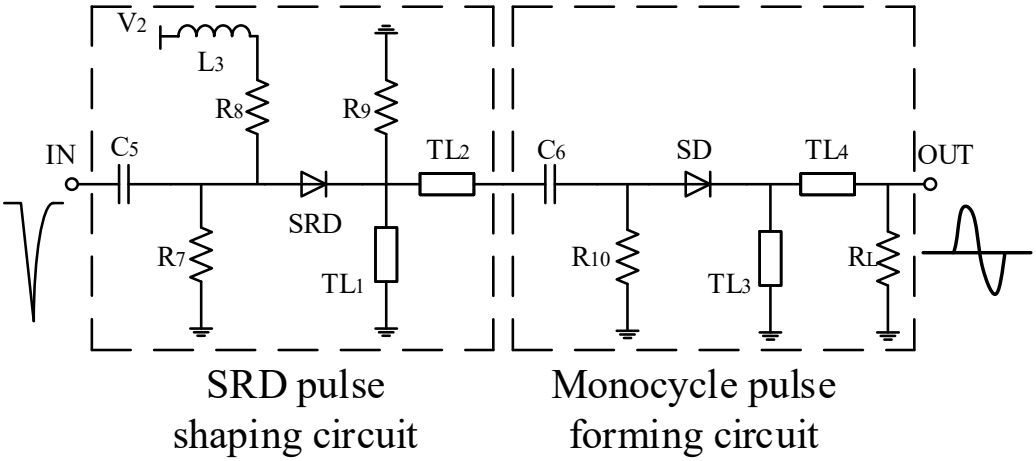


Fig. 3 Circuit diagram of pulser module

(a)SRD pulse shaping circuit

As shown in Fig.3, the SRD pulse shaping circuit is composed of C5, R7, L3, SRD, R8, R9, TL1 and TL2. C5 (270pF) and R7 (20Ω) constitute RC coupling circuit which can increase the output power efficiency [13]. The SRD works as a charge-controlled switch. When there is no driver pulse, SRD is in conductive state. Meanwhile, V2 (1V) recharges SRD via L3 (100uH), R8 (68Ω) and TL1, R8 determines the value of the charging current. Whereas when there is a driver pulse, the SRD won't turn into cutoff state until the stored charge in the conductive state consumed completely by the reverse driver pulse and the time of the transient from the conductive to cutoff state is quite rapid, so we can obtain a step pulse at the terminal of the SRD. Afterwards, this pulse divides into two other step pulse upon arriving at the transmission line TL2, which then propagate to the delay line TL1 and the transmission line TL2. The step pulse traveling toward TL1 is reflected back and eventually combines with the other step pulse to form a Gaussian pulse [9]. The width of the resultant pulse tg is given by the following expression:

$$tg=2L/vp. \quad (1)$$

Where vp is the phase velocity along the delay line TL1 and L is the length of TL1. In this progress, the resistance R9 (330Ω) is used to match the impedance between the SRD pulse shaping and the monocycle pulse forming circuit.

(b)Monocycle pulse forming circuit

The monocycle pulse forming circuit is composed of C6, R10, SD, TL3 and TL4. C6 (20pF), R10 (10KΩ) and SD constitute RC decoupling circuit which can reduce the ringing level of the output pulse [13]. The direct coupling of the two distributed delay lines TL1 and TL3 may cause problem of backward transmission of the reflected impulse from the second to the first delay line, forming large ringing on the output pulse. Therefore, a backward decoupling circuit is needed to reduce the backward coupling effect. The function of TL3 is the same as TL1, the negative pulse reflected back from TL3 eventually combines with the positive pulse at the load RL (50Ω). So we can obtain a monocycle pulse at the output terminal.

3. Experiment and Discussion

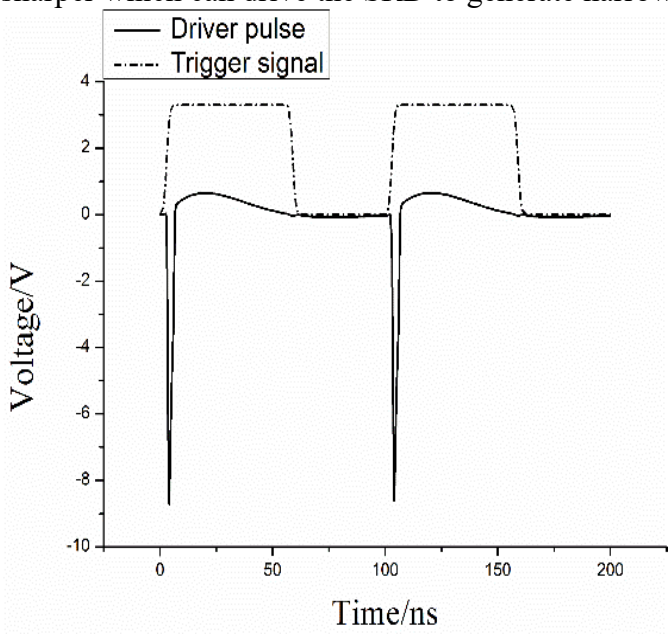
Through multiple simulation tests, the value of the main components selected in the pulse generator circuit are shown in table1.

Table 1 Main components of the pulse generator

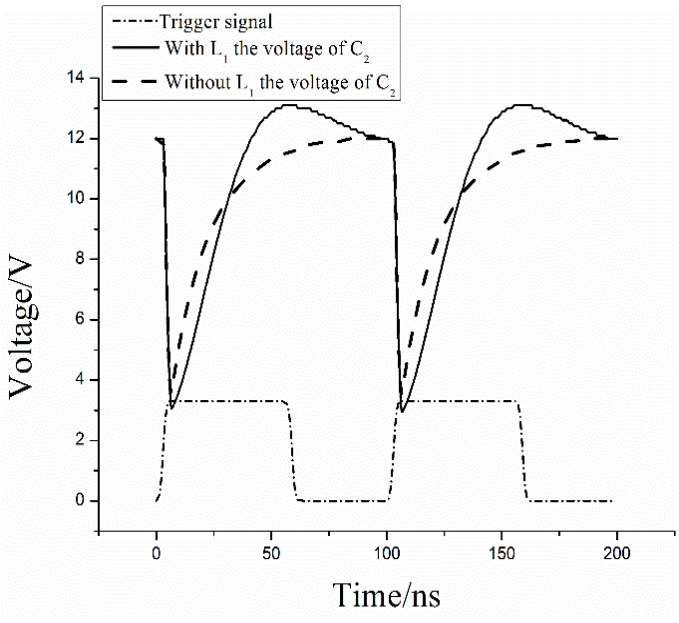
Component	Type	Remark
Q1,Q2	BFP450	/
SRD	MP4023	/
SD	HSMS2860	/
TL1,TL3	Microstrip line	W=1mm, L=12mm
TL2	Microstrip line	W=2mm, L=6mm
TL4	Microstrip line	W=2mm, L=15mm
Substrate	FR4, εr=4.2, tanD=0.033, H=1mm, T=0.035mm	
Trigger signal	0-3.3V, 10MHz, Square signal, rise time(fall time)=6ns	

3.1 Simulation Results of the Driver Module

The driver module is simulated in the software ADS (2016). The result shown in Fig.4 (a) indicates that the driver pulse whose amplitude is about 8.6V and the pulse rise time (fall time) is less than 2ns. Comparing with the trigger signal, the pulse amplitude is much larger and the edges is much sharper which can drive the SRD to generate narrow pulse more effectively.



4 (a) Driver pulse



4 (b) Voltage of C2

Fig.4 Diagram about the waveform of the driver module

To illustrate the function of L1 mentioned in 2.1 (b) more intuitively. We give the simulation result about the voltage of C2 before and after introducing L1 in the driver module, as shown in Fig.4 (b). The result indicates that after introducing L1, the peak voltage of C2 becomes larger and the time of

the peak voltage is much smaller than before. So, the L1 plays an important role in accelerating the charging progress and enhancing the voltage of C2 as described in paper [11].

3.2 Simulation Results of the Pulse Generator

The whole pulse generator circuit is simulated in the software ADS (2016). The result shown in Fig.5 indicates that the monocycle pulse whose pulse full width is about 600ps and pulse amplitude is about 6.3V peak-to-peak with -24dB ringing level and good symmetry. Besides, the pulse generator can work steadily under the condition of 10MHz trigger signal excitation.

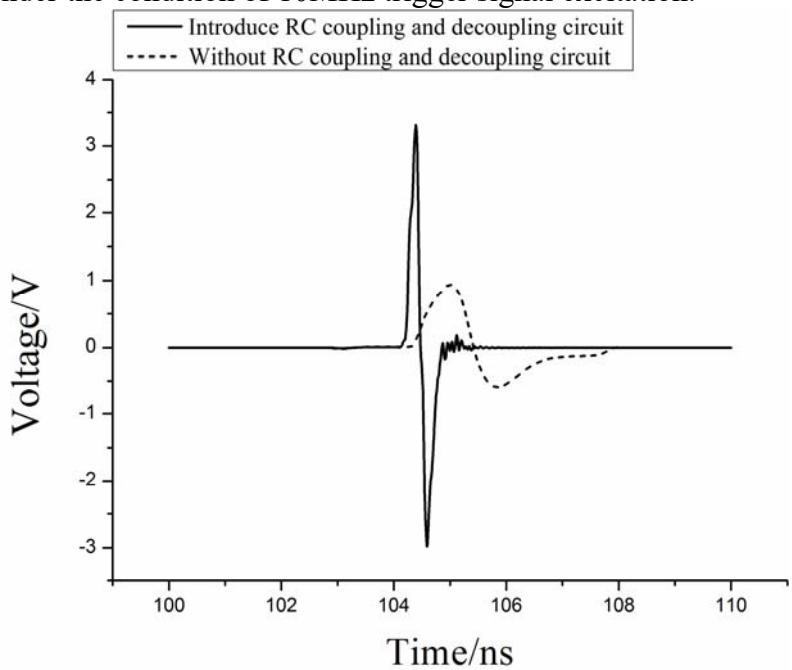


Fig.5 Diagram about the monocycle pulse of the proposed pulse generator

To demonstrate the importance of the RC coupling and decoupling circuit mentioned in 2.2 (a) and 2.2 (b) more intuitively. We give the contrast about the output monocycle pulse before and after introducing RC coupling and decoupling circuit in the pulser module, as shown in Fig.5. The result indicates that the pulse width is much wider and the amplitude is much lower without using RC coupling and decoupling circuit. After introducing the two structure, the pulse has much narrower duration and the amplitude becomes much higher. So introducing RC coupling and decoupling circuit is useful for increasing the output power efficiency and reducing the distortion of output pulse as explained in paper [13].

3.3 Fabrication of the PCB Board

We have fabricated the circuit on the FR4 substrate, as shown in Fig.6. In the experiment test, the driver module can work well, but the pulser module is still needed to be tuned and the layout method is also needed to be improved.

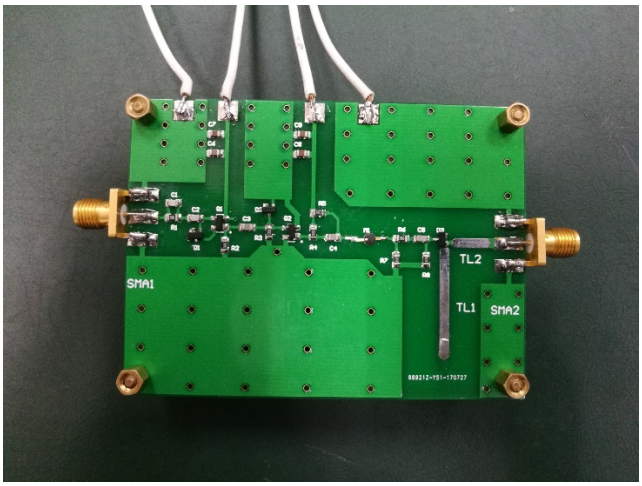


Fig.6 Diagram of the pulse generator PCB board

Furthermore, in order to evaluate the performance of the proposed pulse generator, a comparison of various UWB pulse generator simulation results which have been reported in the references is shown in table 2.

Table 2 Comparisons with pulse generations in literatures

Reference	Input signal		Output pulse			
	Repetition	Voltage	Shape	Voltage	Duration	Devices
[1]	?	?	Gauss	-11.2V	890ps	Avalanche Transistor
[2]	1-100MHz	4V	Mono	680mV	355ps	SRD
[7]	1 MHz	?	Gauss	-6.7V	400ps	Avalanche Transistor
[8]	1 MHz	3.3V	Gauss	2.25V	902ps	Avalanche Transistor
[9]	10 MHz	?	Mono	2V	330ps	SRD
[10]	10 MHz	?	Mono	400mV	300ps	SRD
This work	10 MHz	3.3V	Mono	6.3V	600ps	Avalanche Transistor + SRD

As shown in table 2, the pulse generator proposed in this paper can generate monocycle pulse whose duration is relatively small and the amplitude is kept at a high level. Therefore, this generator is much more suitable for the UWB applications.

4. Conclusion

In this paper, we have presented a high-performance ultra-wideband monocycle pulse generator. The main modules of the generator were described in detail and analyzed by a transient simulator in the RF software ADS. Innovatively, we utilize the avalanche pulse to drive the SRD, and finally we obtained the monocycle pulse whose amplitude is 6.3V and the pulse full width is 600ps with -24dB ringing level. The proposed generator proves to be structurally compact and low cost, but the layout method is still needed to be improved in the future. With the good performance such as high amplitude and low ringing level, the generator can be introduced in the fields of ground penetrating radar, see-through-wall imaging and so on.

References

[1] Wang Q, Tian X, Liu Y, et al. Design of an Ultra-Wideband Pulse Generator Based on Avalanche Transistor[C]// International Conference on Wireless Communications, NETWORKING and Mobile Computing. IEEE, 2008:1-4.

[2] Kamal A, Bhattacharya A, Tamrakar M, et al. Low-ringing and reduced-cost step recovery diode based UWB pulse generators for GPR applications [J]. Microwave & Optical Technology Letters, 2014, 56(10):2289-2294.

[3] Maaref N, Millot P, Ferrières X, et al. Electromagnetic Imaging Method Based on Time Reversal Processing Applied to Through-the-Wall Target Localization[J]. Progress in Electromagnetics Research M, 2008, 1:59-67.

[4] Yang Y, Fathy A E. Development and Implementation of a Real-Time See-Through-Wall Radar System Based on FPGA [J]. IEEE Transactions on Geoscience & Remote Sensing, 2009, 47(5):1270-1280.

[5] Kim H, Joo Y, Jung S. A Tunable CMOS UWB Pulse Generator[C]// IEEE 2006 International Conference on Ultra-Wideband. IEEE, 2015:109-112.

[6] Sim S, Kim D W, Hong S. A CMOS UWB Pulse Generator for 6–10 GHz Applications [J]. IEEE Microwave & Wireless Components Letters, 2009, 19(2):83-85.

[7] Guo Y, Zhu G, Zhou Z. A novel design and implementation of sub-nanosecond sampling pulse generator for ultra-wideband equivalent sampling receiver[C]// International Conference on Computing, Communication and NETWORKING Technologies. IEEE, 2014:1-5.

[8] Zhang J, Zhu H, Qiao Y, et al. Design and Analysis of Guided Wave Radar Level Meter Transmitter Circuit[J]. Computer & Digital Engineering, 2014.

[9] Lee J S, Nguyen C, Scullion T. New uniplanar subnanosecond monocycle pulse generator and transformer for time-domain microwave applications [J]. IEEE Transactions on Microwave Theory & Techniques, 2001, 49(6):1126-1129.

[10] Han J, Nguyen C. A new ultra-wideband, ultra-short monocycle pulse generator with reduced ringing [J]. Microwave & Wireless Components Letters IEEE, 2002, 12(6):206-208.

[11] Cui Y, Zeng Y, Huang N. Design of Differential Gauss UWB Pulse Generator [J]. Semiconductor Technology, 2008.

[12] Zhang J, Raisanen A. A new model of step recovery diode for CAD[C]// Microwave Symposium Digest, 1995. IEEE MTT-S International. IEEE, 2002:1459-1462 vol.3.

[13] Han J, Nguyen C. On the development of a compact sub-nanosecond tunable monocycle pulse transmitter for UWB applications [J]. IEEE Transactions on Microwave Theory & Techniques, 2006, 54(1):285-293