Research and Design of Low-Frequency RFID Tag Chip Based on FPGA

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Abstract. For the limitation of the low-frequency tag chip, a new type of low-frequency radio frequency identification (RFID) tag chip is designed based on the field programmable gate array (FPGA) platform. During the research, FPGA is selected as the microprocessor, with the RF circuit, taking active RFID work to generate signal and process rapidly. The peripheral part of the processor uses the discrete components to design the hardware circuit to achieve the modulation and demodulation function of the coupling signal. Before the digital signal arrived at the RF, it needs to be processed by the internal logic of FPGA. The results reveal that the entire chip system shows a good reading and writing ability and recognition distance, highly restitutes the modulating signal which has not obviously coupling signal, and the simplified instruction optimizes the process, enables the chip to be widely used in more rapid industrial applications.

1. Introduction

RFID (Radio Frequency Identification), is a non-contact automatic identification technology, use radio frequency signals through spatial coupling (alternating magnetic field or electromagnetic field) to achieve contactless information transfer. It is widely used in schools, public transportation, access control, electronic wallet, medical treatment and other fields with its features of non-contact, high reliability, good safety performance, no need of human intervention, workability and any harsh environment [1]. Low-frequency RFID tags generally work between120KHz to 134 KHz, in this paper, the chip operating at 125 KHz, in addition to the impact of metal materials, generally, low-frequency can be passed through any material without reducing its reading distance [2]. RFID technology has been widely used in the low-frequency application and promotion. And the market for low-frequency tags are mostly read-only, cannot write data. With the progress of science and the continuous development of industrialization, various fields have raised new requirements and challenges for low-frequency RFID tags. The read-only tags cannot meet the market demands.

This paper designs a low-frequency RFID tag chip base on FPGA and simplifies the system Instruction. The rich resource and powerful functions of FPGA ensure the stability of the system [3]. The program designed dedicated RF circuit, with 125 KHz coil. It uses active operation mode, without obtaining external supply voltage, which saves cost and ensure the efficiency of the chip operation.

2. Overall Design of System

The design scheme mainly consists of field programmable gate array, RF circuit, EEPROM and 125 KHz antenna. The overall structure shown in Fig.1. Among them, the microprocessor selects ALTERA company's board and the 24LC04B model electrically erasable and programmable EEPROM inside the floor board as the read-write memory, which is a memory chip that data will not be lost after power down.

The microprocessor includes a decoding module, an encoding module, a CRC checking module, an anti-collision module and a main control module. The RF circuit module includes an ASK demodulation module and a load modulation module. The data transport through 125 KHz Coil antenna between tags and external reader by coupling communication. External Reader can read or

write to the tags. The write operation means that coupled signal by coil processed by the ASK demodulation module in the RF circuit module and then transmitted to the FPGA via the interface. Microprocessor internal decoding module according to the ISO18000-2 protocol processes and verificates digital signal timely. The data which meet the protocol requirements are written to the EEPROM memory at the appropriate address via the IIC bus interface to complete the write operation. Reading operation is the FPGA take the initiative to encode the information in the EEPROM and the encoded signal is loaded onto a 125 KHz carrier via load modulation circuit.
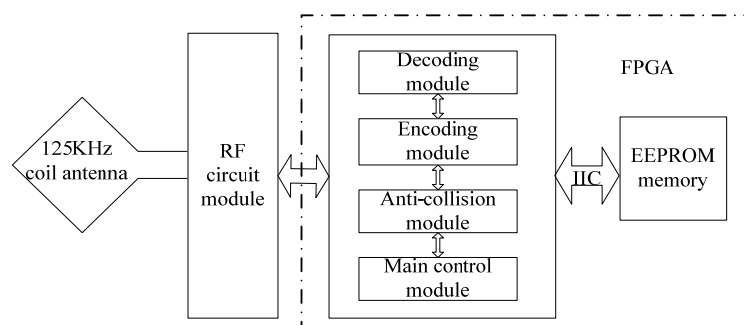
Fig.1 Architecture of chip

2.1 RF Circuit Design

Low-frequency RFID has no dedicated RF circuit chip to achieve wireless communications. Therefore, this paper designs a set of dedicated low-frequency RF circuit with discrete components and uses microprocessor as core with peripheral circuit which includes the EEPROM module, power module, ASK demodulation module and load modulation module, the structure shown in Fig.2.
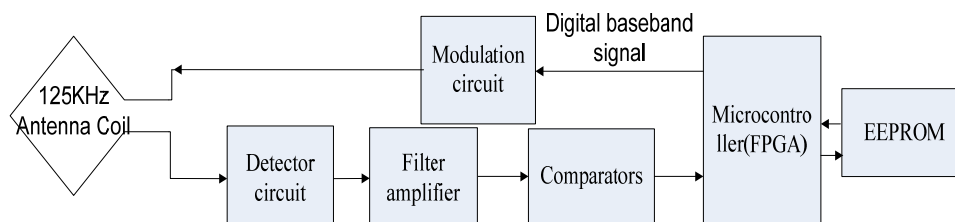
Fig.2 Schematic diagram of the chip

Microprocessor has rich logic resources and pin interfaces, while meeting the chip system's requirements, it costs less, costs effective and configures flexible [4]. RFID tag data can be conveyed bi-directional in the way of half-duplex or full-duplex between the reader and RFID card. FPGA uses the internal PLL to generate 125 KHz clock signal and generate a unique string of data within the memory. The signal is encoded according to the encoding structure specified in the ISO 11784/11785 protocol [5,6]. And it is used to drive the NMOS switch to adjust the voltage of the tag's resonant tank according to the beat of data. The amplitude of the voltage across the reader coil changes. After the reader demodulates the data of the identification tag, the related information is extracted and transmitted to the host computer. When the reader needs to send other operations to the label, the tag transponder induces reader signal by coupled coil. ASK circuit demodulated signal and sent to the microprocessor's decoding module. The main module generates corresponding data which meet the command to the reader.

Fig.3 shows part of the ASK demodulation circuit with discrete devices. Envelope demodulation does not need to extract the carrier signal, is widely used in RFID tag chip[7]. The ASK demodulation circuit consist of the detector circuit, filter amplifier and hysteresis comparison circuit. The HT7553 low-power linear regulator provides a stable 3.3V operation for the circuit. The BAS70-07 diode obtained transponder signal by envelope detection. And its low junction capacitance, high frequency and high sensitivity and other characteristics brought great convenience to the entire circuit. After the

detection signal is transmitted to the second-order full-feedback Butterworth active low-pass filter composed of the AD8052 device, it has good effect for filtering the noise signal. The AD8052 allows amplification of a common mode voltage of 1.5V up to 3.3V. The purpose is to amplify the modulation depth and to enable the carrier signal to be better restored. Voltage comparator selected LM293, a wide operating voltage and can be directly connected with the TTL logic circuit, what makes the decoding of the microcontroller easier and faster.
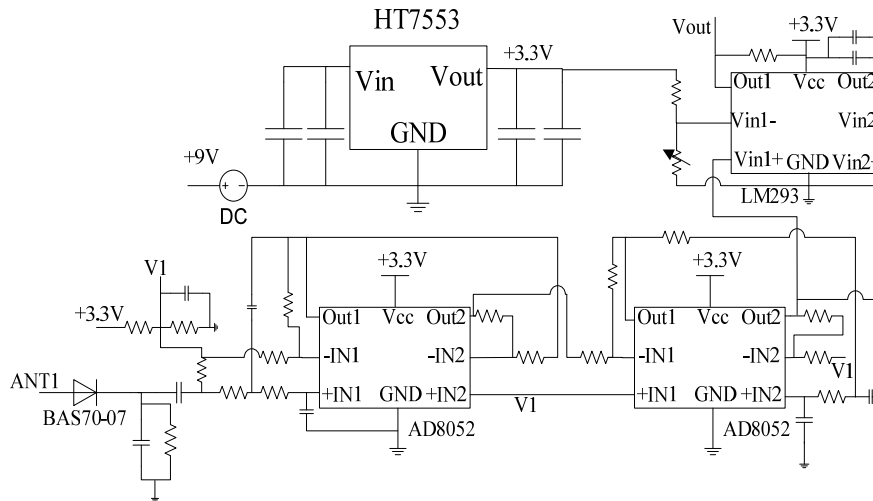
Fig.3 ASK demodulation part of the circuit diagram

Fig.4 shows a partially loaded modulation circuit. Load modulation is the way that tags transport data to the reader [8]. Use BM28N10 as a switch, ID number control the NMOS load modulation network.
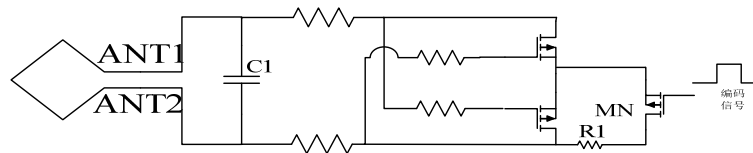
Fig.4 Load modulation part of the circuit diagram

2.2 Digital Part Design

The digital circuit is the "heart" of the entire RFID tag. The main function of the digital circuit is to decode and interpret commands, flip state, read and write memory, and code output signal. The main modules included in the digital circuit are the main state machine, receive, transmit, and memory interface circuits. The receiving part is used to receive the instruction sent by the reader, decode the instruction, and extract the instruction parameters to provide input to the main state machine processing instruction. The sending part is responsible for the response to the instructions, including data packing and coding. Memory interface is responsible for controlling the memory read and write, erase function timing, to ensure memory is working properly. Cyclic Redundancy Check (CRC) is the flag to determine whether the received instruction data is complete and valid, and to ensure the integrity of the instruction data. According to the ISO18000-2 communication protocol [9], as shown in Table 1 and Table 2, the command and response contents are included between the frame header SOF and the frame end EOF. Each command sent by the reader and the response returned by the tag transponder should be carried out CRC check.

Table 1 Command Format

	5bits	6bits	8	n	16	
SOF	Flags	Command	Parameters	Data	CRC	EOF

Table 2 RESPONSE Format

	1bits	n	16	
SOF	Error	Data	CRC	EOF

The entire digital system part of the workflow shown in Fig.5. The work process is as follows: The working low-frequency RFID reader will always send 125KHz carrier. After the system power-on reset, the original ID serial number of the system will be sent to the reader carrier through the load modulation circuit. This is the tag features, in the coupling field has been actively sending data. Once the decoding module detects the SOF header, the data between header and end of the frame will be saved immediately. The digital filter in the decoding module ensures the accuracy of the decoded information. At this point, the CRC verification module is activated to Verify the correctness of the command. The CRC check fails, which means the command sent by the reader is unsuccessful or has an error. The tag will return an error response to the reader and wait for the next command. If CRC check is successful and the command is identifiable, the tag takes a read or write message according to the decoded command. The read operation is the tag returns the information requested by the reader. Write operation means that the data included in the command is written to memory. The read operation includes a inventory command, which is a built-in anti-collision command format and a unique read method for the presence of multiple labels in a coupling field. Upon receiving the inventory command, all tags in the field execute an anti-collision algorithm, and the reader selects the tag which meet the requirements of the command and reads its internal information. In this system, the simplified instruction set makes the whole system work more smoothly and conveniently, and can be better applied to the fast industrial applications. In order to be able to read quickly, the specific parameters in the command are designed to be used in practical applications. After executing the command, the optional items are omitted in the transmission, only the necessary parameters to be transmitted. For example, the dedicated instruction in this instance is applied to the industrial field. If the received command indicates that the tag is used in the industrial field, the anti-collision enable signal is automatically pulled down and the transmitted data is omitted CRC check portion to accelerate the communication speed.
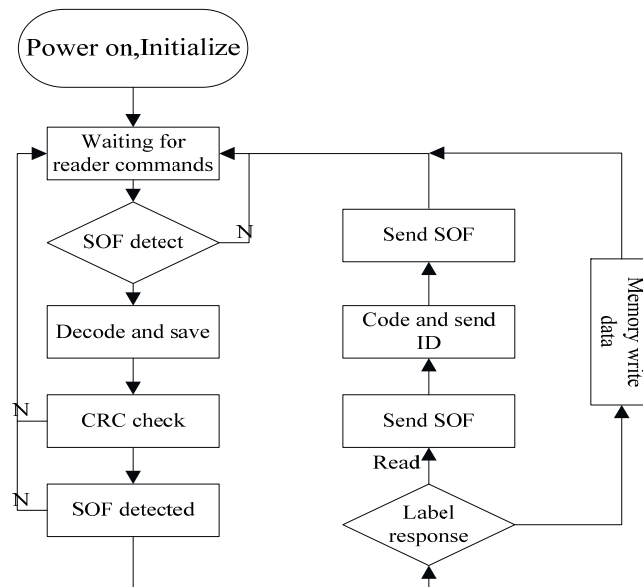

Fig.5 Digital part of the working flow chart

3. Simulation

Using verilog hardware description language to write programs and test, with Modelsim functional simulation, verification in the FPGA development board. Fig.6 shows the data waveform

formed on the carrier sent by the reader after the system decoding, with high recognition. Fig.7 for the simulation of the decoding waveform, Main_in is the RF input signal, clk_1m is the decoding module clock signal, rxd is the filtered signal of the input signal, data_val_r is the data valid flag, sof_found is the sign of start bit, code_out is decoded data. Fig.8 and Fig.9 show that Write 8'b0000_1110 to memory and read it correctly.
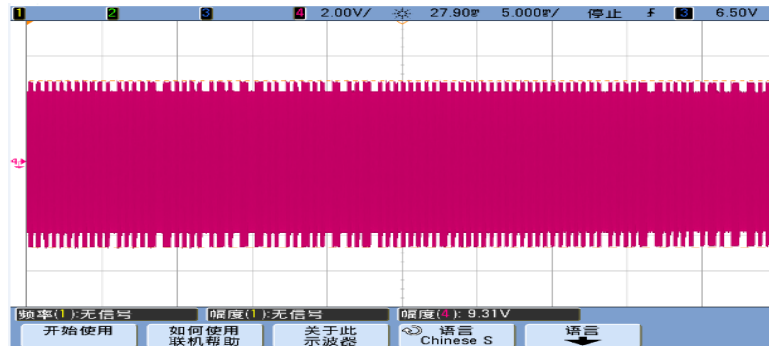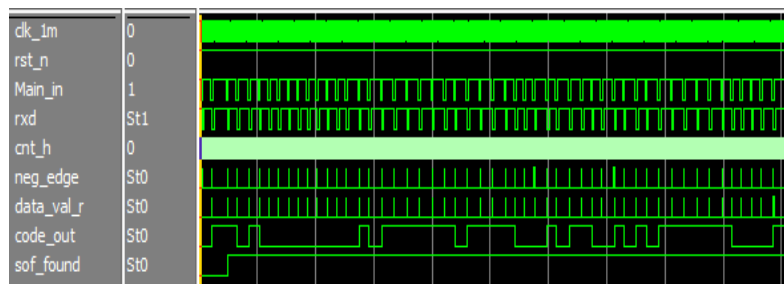

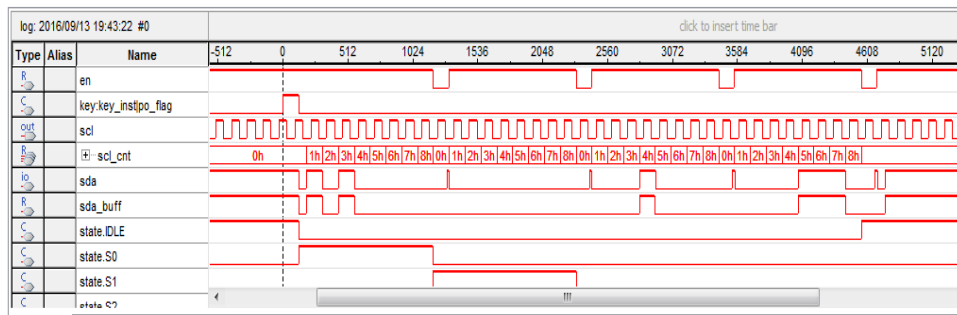Fig.6 The waveform after the load modulation

Fig.7 Decoding waveform
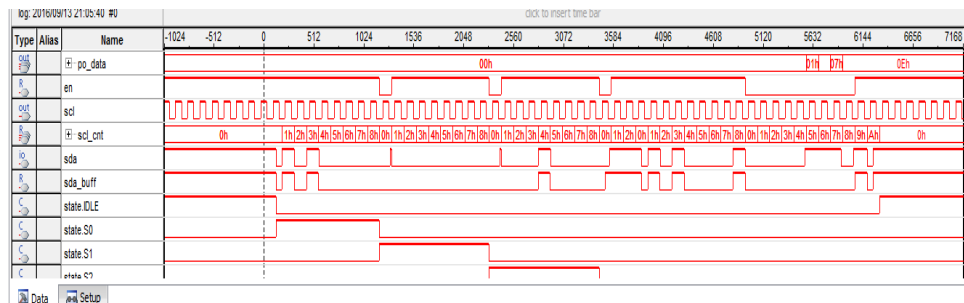

Fig.8 Write data

Fig.9 Read data

4. Conclusion

The paper presents a research and design of a low-frequency RFID tag chip based on FPGA, and explains the whole design flow and working principle. The stable and low-cost RF circuit designed by discrete components enhances the recognition effect and obtains accurate signals. FPGA powerful

data processing capabilities and parallel control capabilities to achieve real-time and efficient RF circuit data. Optional anti-collision algorithm consisting of simplified instruction set more suitable for use in the field of industrial control, promote the development of industrialization.

References

[1]. Lv Xiaoyan. General low-frequency RFID reader research [D]. Hangzhou University of Electronic Science and Technology, 2012.

[2]. Lin Changlong, Sun Xinzhuo, Guo Zhenyi. Design and Analysis of Low Frequency and Low Power Passive RFID Analog Front End [J] .Chinese Journal of Semiconductors, 2015, 40 (9): 653-657.

[3]. Du Ping, Jing Weiping. A Low Frequency RFID Wafer Parallel Test System Design [J]. Semiconductor Technology, 2016 (11): 864-868.

[4]. Zhang Huilei, Jing Weiping. Design of RFID Wafer Parallel Test System Based on FPGA [J] .Chinese Journal of Semiconductors, 2015, 40 (11): 866-871.

[5]. ISO/IEC11784, Radio-frequency dentification of animals-code structure [S]. 1996.

[6]. ISO/IEC11785, Radio-frequency dentification of animals-technical concept [S]. 1996.

[7]. Kong Lingrong. A kind of ASK demodulation circuit suitable for low-frequency RFID tags [J]. Computer & Digital Engineering, 2016, 44 (6): 1171-1175.

[8]. Lin Tianliang, Chen Xi. Design and Implementation of Wireless RF Transponder Based on Load Modulation Theory [J]. Laboratory Research and Exploration, 2015, 34 (8): 112-114.

[9]. ISO/IEC 18000-2, Information technology-Radio frequency identification for item management[S].2004.