Fault Location of Electrical Equipment Based on Rough Set Fusion Grey Correlation Degree

Wang Ziyu

North China Electric Power University, Beijing, China

Keywords: fault diagnosis; fault test; fault location; electrical equipment

Abstract: In complicated and bad natural environment, the performance of electronic system may be easily affected by the environment, go wrong and result in abnormal operation. In the complicated environment like deep space and deep sea, if the electronic equipment after break down cannot be repaired in time, it will cause serious loss. However, the fault self-repairing technique proposed based on hardware evolution can realize self-repairing of fault. The paper firstly expounds the basic theory of hardware evolution and introduces foreign and domestic situation of fault self-repairing based on hardware evolution in details. Then, it explains important procedures in fault self-repairing and points out the existing problems and improvement direction. Fault self-repairing based on hardware evolution has very broad prospect and great engineering application value.

1. Introduction

Traditional electronic circuit structure is fixed and invariable. As the acceleration of information construction, electronic system is widely used for electronic equipment. It mostly takes large-scale and super large-scale digital integrated circuit as the subject and the core is field programmable gate array (FPGA). When these electronic systems are in the complicated and variable environment like sand dust, high/low temperature, strong electromagnetic field, the performance of digital integrated circuit may be affected, go wrong and thus reduce the function of electronic equipment, and even cause serious casualties and property loss. Further, a series of problems shall be urgently solved so as to enhance the survival ability of electronic system in bad environment and ensure continuous and normal operation of digital system.

2. Major Self-Repairing Techniques of Electronic Circuit Fault Based on EHW

Combining the advantages of hardware and software, FPGA develops “deformation system” that is reassembled on chip. Some functions of hardware can be configured on chip, so software is designed for hardware simulation. In this way, the “firmware” of FPGA is reassembled and used for simulated different types of hardware. When realizing self-repairing of digital circuit fault, as is shown in Fig.1., fault detection, fault location, fault isolation, redundancy design and evolutionary algorithm are indispensible. They form a complete system. Fault self-repairing of digital system has become a hot topic in fault diagnosis research field.

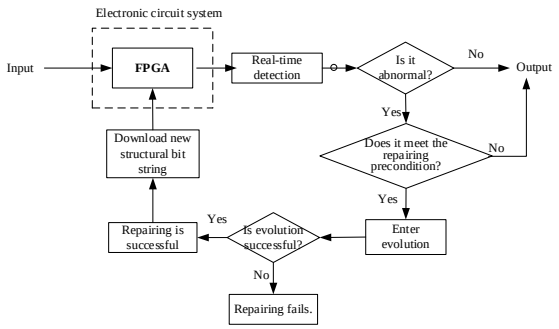

Fig.1. Basic flow chart of fault self-repairing realized in the hardware evolution

3. Fault Diagnosis Technique

Fault diagnosis of digital circuit mainly tests the function, sequence relationship, logic relationship. According to the different characteristics of combinatory logic circuit and sequential circuit, the used test methods are different. Fault type of digital circuit mainly includes constant fault, bridging fault, transient-state fault and time lag fault. Now, constant fault is mostly studied.

3.1 Generation of test vector

Based on the difference between combinatory circuit and sequential circuit, there is difference when generating test vector. In the test of combinatory logic circuit, the common methods include pseudo exhaust testing, boolean difference method, characteristic analysis method, and casual function analysis method. The related algorithm can be classified as D cube, D algorithm, PODEM algorithm and FAN algorithm of logic function; the test method of sequential circuit mainly includes extended D algorithm and nine value algorithm, etc.

3.2 Fault location technique

Traditional FPGA diagnosis method includes boundary scanning technique, but boundary scanning technique cannot locate the logic cell, and the hardware expenditure is high. Increasing boundary scanning by virtue of chip can shorten the test engineering of manufacturing industry and reduce the launch time, but it may prolong the design time.

Various location techniques have appeared in logic cell fault location. One is configuring circuit for the tested cell and drawing it to IOB port directly when detecting fault of a very few single CLB; however, when the quantity of tested CLB is too large, the method based on array, method based on exclusive-OR gate cascade circuit, method based on AND-OR gate cascade circuit, and Build-in Self-test (BIST) method are proposed. The circuit configuration of BIST is complicated, and the configuration may fail; while method based on exclusive-OR gate cascade circuit and method based on AND-OR gate cascade circuit can detect fault at the port, but it can only detect half of CLBS after configuration once and needs to use at least half of CLBS to transmit fault.

3.3 EHW technique

Studying EHW mainly studies evolutionary algorithm. Firstly, the internal structure and coding way of FPGA should be studied. The structure of programmable logic device (PLD) is decided by the structural bit string. Structural bit string can be deemed as the chromosome in evolutionary algorithm and the design of hardware function can be completed through evolutionary algorithm. Fig.2. is the internal structure diagram of PLD. The circuit function expression is: $Y1 = AB + \overline{C}E + \overline{B}D + ACE$.

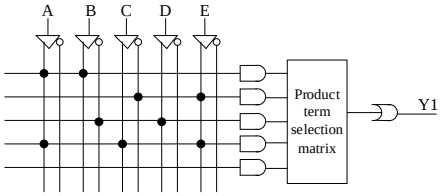

Fig.2. PLD structure diagram

Fig.3. is the basic schematic diagram of EHW. It mainly codes the programmable circuit structure, carry out evolutionary operation of code according to a certain constraint condition and get code with high fitness value. At last, it decompiled the code to topological structure of circuit.

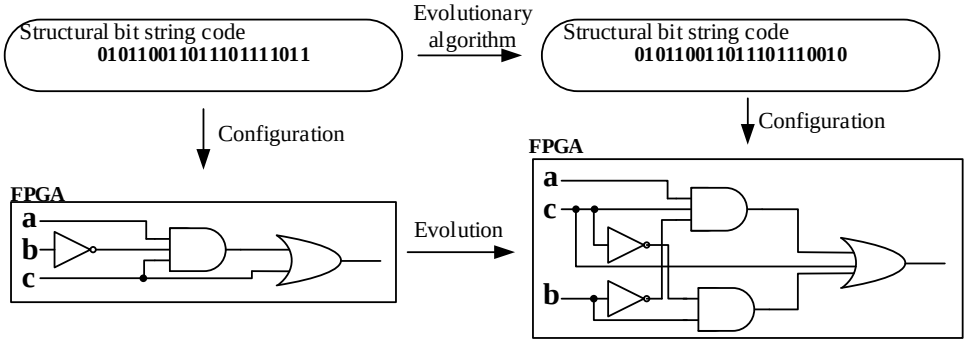

Fig.3. Basic schematic diagram of hardware evolution

4. Conclusion

At present, fault diagnosis technique is mature increasingly and difficult to innovate. Most researches focus on integrated application of diagnosis techniques and research on using hardware evolution for fault self-repairing is deep, but it is at starting stage in China. Limited by scientific research condition, research on related technology is still at theoretical research stage. The research is single, mainly focuses on improvement of evolutionary algorithm without substantial leap. Digital circuit self-repairing technique based on EHW is the organic combination of evolutionary algorithm and PLD. It changes its own circuit structure according to the change of external environment so as to realize the function requirement of target circuit. The technique will certainly develop forward in each field, especially has broad prospect in national defense and military field. Combination of EHW technique and fault diagnosis and expanding technical approach of fault self-repairing will become research topic.

References

[1] Malarkodi, M.P., Arunkumar, N., Venkataraman, V. Gabor wavelet based approach for face recognition (2013) International Journal of Applied Engineering Research, 8 (15), pp. 1831-1840.

[2] Stephygraph, L.R., Arunkumar, N.Brain-actuated wireless mobile robot control through an adaptive human-machine interface (2016) Advances in Intelligent Systems and Computing, 397, pp. 537-549.

[3] Lv, Z., Halawani, A., Feng, S., Li, H., & Réhman, S. U. (2014). Multimodal hand and foot gesture interaction for handheld devices. ACM Transactions on Multimedia Computing, Communications, and Applications (TOMM), 11(1s), 10.

[4] Yizheng Chen, Fujian Tang, Yi Bao, Yan Tang, *Genda Chen. A Fe-C coated long period fiber grating sensor for corrosion induced mass loss measurement. Optics letters, 41(2016), pp. 2306-2309.

[5] Arunkumar, N., Jayalalitha, S., Dinesh, S., Venugopal, A., Sekar, D. Sample entropy based ayurvedic pulse diagnosis for diabetics (2012) IEEE-International Conference on Advances in Engineering, Science and Management, ICAESM-2012, art. No. 6215973, pp. 61-62.

[6] Yijiu Zhao, Yu Hen Hu, Jingjing Liu. Random Triggering-Based Sub-Nyquist Sampling System for Sparse Multiband Signal. IEEE Transactions on Instrumentation and Measurement. 2017; vol. 66, No.7: 1789-1797.