ATLANTIS PRESS
Advances in Intelligent Systems Research (AISR), volume 150
2017 International Seminar on Artificial Intelligence, Networking and Information Technology (ANIT 2017)

A fast construction method for VLSI power and ground pin assignment

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Keywords: signal integrity, pin assignment, prior knowledge, construction method

Abstract. In this paper, a fast pin assignment optimization method is proposed for improving signal integrity performance of VLSI package. This performance is evaluated by two cost function. Some other methods based on heuristic algorithm can find a good solution for pin assignment problem. Since the solution space is of high dimension, those algorithms require a large time consumption. The proposed pin assignment construction method is guided by the prior knowledge about the optimal solution of pin assignment. It generates a solution by directed construction. Experimental results show that the quality of solution produced by proposed method is better than that by heuristic algorithm and the time consumption is practically negligible.

1 Introduction

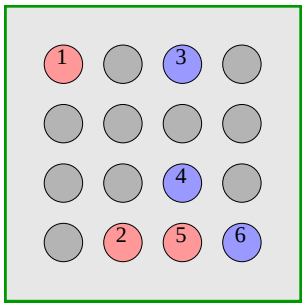
With the rapid increase in VLSI performance and the associated enhancement in their functions, more and more functional circuits are integrated into a single chip. Signal integrity problem due to power and ground (P/G) pin arraignment turns into a critical problem in VLSI designing[1].

Since the pin assignment problem is NP-complete [2] which conventional optimizer cannot solve. There has been some work in pin assignment problem with heuristic algorithm being implemented. In [3], the inductance matrix $\boldsymbol{L}$ of the package are extracted to calculate the ground noise voltage, then the optimization problem is to minimize it. Recently, [4] has proposed two cost function models to evaluate the mutual inductance and return path quality. They are combined into a single fitness function and the problem is also to minimize it. Heuristic algorithms such as genetic algorithm (GA) and simulate anneal (SA) are used in [4][5]. These algorithm works well but consumes too much time for iterative computation. However, the optimal solutions are regular. With this prior knowledge, it's possible to find a relatively good solution in an extraordinarily short time. This paper focus on reducing time consumption when dealing with large-scale packages.

2 Preliminary

For a given package (Fig. 1 (a)), all the P/G pin are numbered. A distance matrix $\boldsymbol{D}$ (Fig. 1 (b)) is derived where its element d_{ij} is the distance between pin i and pin j.

If the number of P/G pin is n, $\boldsymbol{D}$ is of $n \times n$ dimension. The elements on its diagonal are replaced with $d_{\max}$, which is larger than any element in $\boldsymbol{D}$ and insure the value of the logarithm is positive. To evaluate the power integrity (PI) and signal integrity (SI) performance of a package, two cost functions are derived [4].



(a) 4*4 Package

$$\boldsymbol{D} = \begin{bmatrix} d_{\max} & 3.16 & 2 & 2.83 & 3.61 & 4.24 \\ 3.16 & d_{\max} & 3.16 & 1.41 & 1 & 1 \\ 2 & 3.16 & d_{\max} & 2 & 3 & 3.16 \\ 2.83 & 1.41 & 2 & d_{\max} & 1 & 1.41 \\ 3.61 & 1 & 3 & 1 & d_{\max} & 1 \\ 4.24 & 2 & 3.16 & 1.41 & 1 & d_{\max} \end{bmatrix}$$

(b) Distance Matrix

Fig. 1 Construction of Distance Matrix

Here M_{sum} is derived for the PI:

$$M_{\text{sum}} = \sum_{i=1}^{N}\sum_{j=1}^{N} a_{ij} \ln\left(\frac{d_{\max}}{d_{ij}}\right) \#(1)$$

where

$$a_{ij} = \begin{cases} -1, & \text{when current between pin i and pin j are in opposite direction} \\ 0, & \text{when i=j} \\ 1, & \text{when current between pin i and pin j are in same direction} \end{cases}$$

And D_{sum} is for SI:

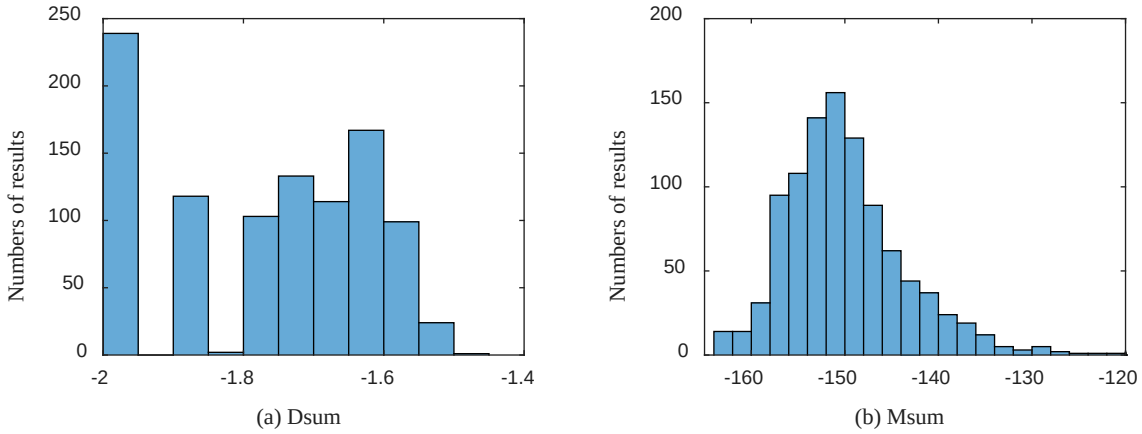
$$D_{\text{sum}} = \text{var}(\boldsymbol{d}_{\min}) - \frac{1}{N}\sum_{j=1}^{N} q_j \#(2)$$

where var denotes to get variance, q_j is the smallest element of the jth column of $\boldsymbol{D}$ and $\boldsymbol{d}_{\min}$ is a vector:

$$\boldsymbol{d}_{\min} = [q_1 \quad q_2 \quad \cdots \quad q_N] \#(3)$$

Because M_{sum} vary in a relatively large range and D_{sum} in a small one. D_{sum} is multiplied by a relatively large weight w. Fitness function f for single object genetic algorithm is equal to the summation of M_{sum} and weighted D_{sum}. In general, a better result has a smaller f value.

$$f = M_{\text{sum}} + wD_{\text{sum}} \#(4)$$



(a) Dsum (b) Msum

Fig. 2 Distribution of Results

To get a clear view of performance, Fig. 2 shows the distribution of M_{sum} and D_{sum}. Here 1000 results of 9×9 package with 25 P/G pins are found by GA and each of them consumes around 3 seconds. Only 8 optimal packages (result in Fig. 3) with the smallest f value is found and the M_{sum} and D_{sum} of the them are -163.92 and -2 respectively.

3 Construction of Pin Assignment

A good return path quality requires a uniform P/G pins distribution. For a 1-dimension package, to get a uniform P/G pin assignment is easy. However, things become complex in a 2-dimension package. The construction procedure is as follows:

1) Initialize scalar d_{shift}, d_{inc}, d_{t} and a vector $\boldsymbol{p}_1$ with alternatively arranged power (P) pins, ground (G) pins and signal (S) pins.
2) Update vector $\boldsymbol{p}_{i+1} = \text{shift}(\boldsymbol{p}_i)$.
3) Update package matrix $\boldsymbol{P}$ with $\boldsymbol{P}_{i\times d_t\text{-th column}} = \boldsymbol{p}_i$ and $\boldsymbol{P}_{(i+1)\times d_t\text{-th column}} = \boldsymbol{p}_{i+1}$.
4) Repeat step 2-3 until $(i+1)\times d_{\text{t}}$ is larger than the number of columns in $\boldsymbol{P}$.
5) Increase d_{shift} and repeat step 2-4 to get $\boldsymbol{P}_1$, $\boldsymbol{P}_2$, $\cdots$, $\boldsymbol{P}_N$.
6) Calculate M_{sum} and D_{sum} for each package.
7) Plot curves of M_{sum} and D_{sum}, select the best package as optimal solution.

In step 1, Parameter d_{inc} is used to control the number of S pin between two P/G pins and d_{t} controls the interval between $\boldsymbol{p}_i$ and $\boldsymbol{p}_{i+1}$. They are initialized according to the ratio between P/G pins and the total number of pins in the package. For a given package, we have:

$$r = \frac{N_{\text{P/G}}}{N_{\text{total}}} \le \frac{1}{d_{\text{inc}} \times d_{\text{t}}} \#(5)$$

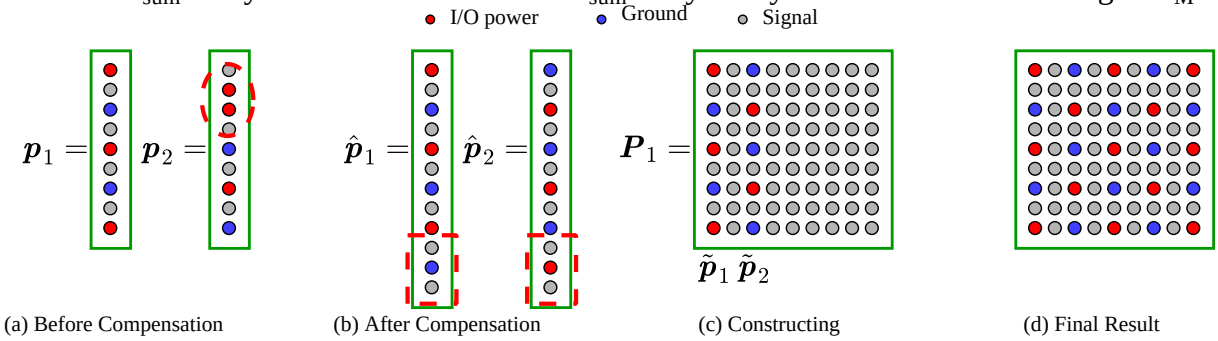
To find the d_{inc} and d_{t} that make r as close to the actual ratio as possible for initializing step. Grid search method can be used.

In step 2, the function $\text{shift}(x)$ works like a shift resister and the shift distance depends on d_{shift}.

In step 3, suppose I_{M} and I_{D} is the period of M_{sum} and D_{sum} respectively. For any package, we have:

$$I_{\text{M}} = 2d_{\text{inc}} \#(6)$$
$$I_{\text{D}} = d_{\text{inc}} \#(7)$$

Because D_{sum} may remain a constant and M_{sum} vary always. N is chosen according to I_{M}.



(a) Before Compensation (b) After Compensation (c) Constructing (d) Final Result

Fig. 3 Construction Procedure of a 9*9 package

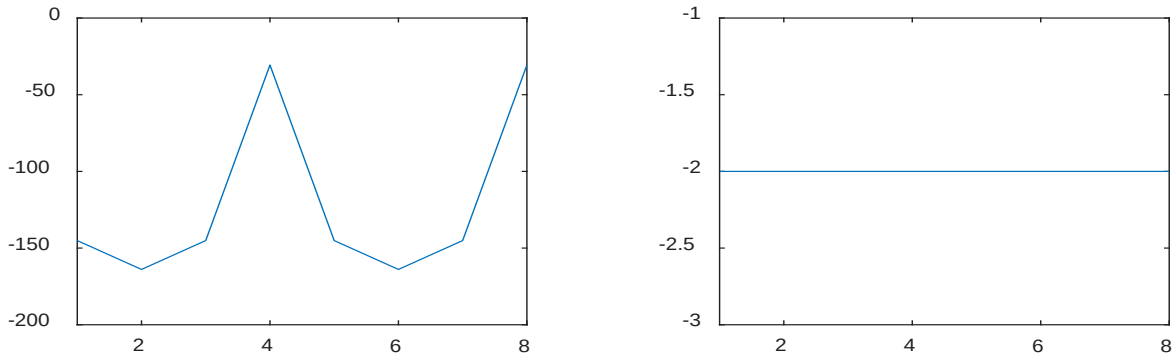
Fig. 3 shows the construction procedure of a 9×9 package with 25 P/G pins, here $d_{\text{shift}} = 2$, $d_{\text{inc}} = 1$ and $d_{\text{t}} = 1$. As show in Fig. 3 (a), the uniform scheme will be broken after shifting directly. To address this problem, some extra pins will be added on the tail of $\boldsymbol{p}$. The number of them can be calculated by

$$N_{\text{add}} = 2d_{\text{shift}} - \text{mod}(l, 2d_{\text{shift}}) \#(8)$$

where l is the length of $\boldsymbol{p}$.

Before shifting, $\boldsymbol{p}_2$ cannot maintain the uniform scheme, but $\hat{\boldsymbol{p}}_2$ can after compensating $\boldsymbol{p}_2$. The extra pins will be abandoned when $\hat{\boldsymbol{p}}_2$ is used to construct $\boldsymbol{P}$.

Several pin assignment schemes will be constructed while changing the shifting distance d_{shift}. Fig. 4 shows the Numeric curves of packages. On this package, D_{sum} remains a constant and M_{sum} changes periodically. This plot shows the best shifting distance is 2. After finishing all steps, the result constructed by proposed method is the same as the best found by GA.

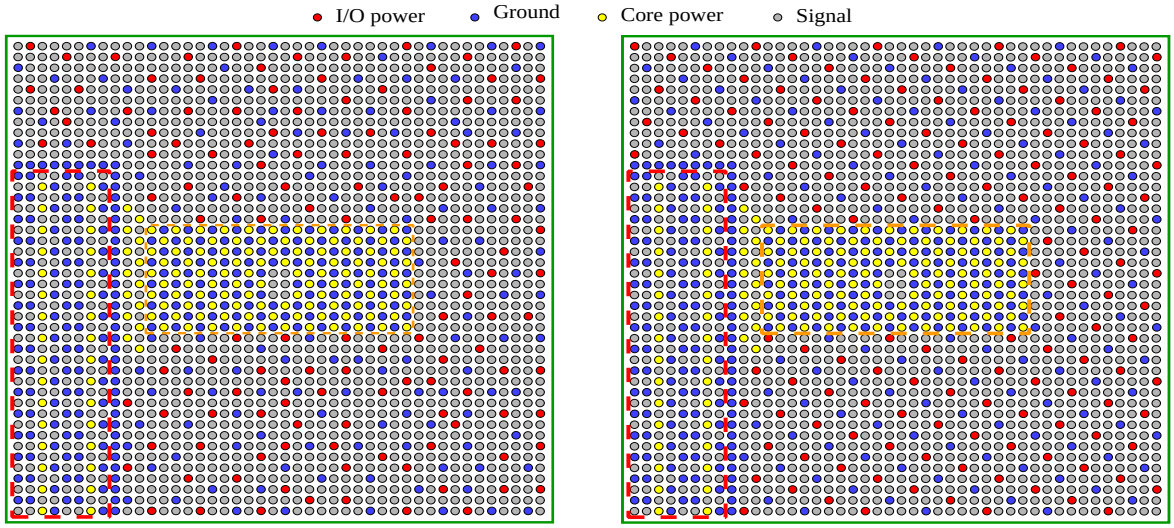


(a) Msum vs Distance (b) Dsum vs Distance

Fig. 4 Numeric Curves of Results

4 Experiment Results

The Xilinx FPGA XC7VX485T is chosen to validate our construction method. The pinout of this device comprises of three parts: core power part (shown in the orange box), differential-pair part (shown in the red box) and GPIO part. Each part is constructed separately. Fig. 5 (a) shows the solution found by GA [4], it takes 30 minutes. In another work [6], it has been reduced to tens of second. Fig. 5 (b) shows another solution constructed by proposed method.



(a) GA (b) Ours

Fig. 5 Experiment Results

The core power part and differential-pair part are the same since they are both small packages. By comparing the GPIO part of each solution. The pin assignment scheme of our solution is more uniform. To make the difference more obvious, a technique called color map assessment [6] is used.

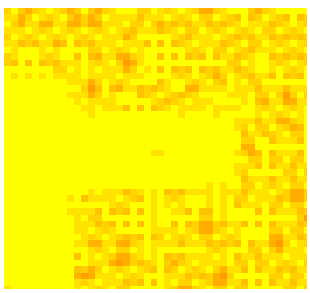


Fig. 6 Colormap of Solutions

Fig. 6 shows the color map of the solutions. In Fig. 6 (a) and (b), light yellow area shows the good return path quality while dark area shows the worst. In Fig. 6 (c) and (d), the blue (cool) area show a negative inductance which means good signal integrity and that of the red(hot) area is poor.

5 Conclusion

In this paper, a fast pin assignment construction method for large-scale BGA package is proposed. It's guided by the prior knowledge of the optimal solution. It's highly efficient in package designing. If there is a need for a further optimal pin assignment scheme, the solutions found by the proposed method can act as the initial solutions in heuristic algorithms for further optimization [7].

Acknowledgement

In this paper, the research was sponsored by the National Natural Science Foundation of China (Project No.61473322). Nature Science Foundation of Guangdong (Project No.2016A030310335) and SYSU-CMU Shunde International Joint Research Institute Major Research Project (Project No.20170106).

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