

# Combined approach for VLSI placement problem

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**Abstract** — The work discusses a stage of electronic computing equipment automated design - VLSI fragments placement. This task belongs to the NP-complex class of problems. The paper presents the statement of the VLSI placement problem. It is proposed an "evolution" - "search" strategy. A new search architecture based on the proposed strategy is constructed. The principal difference of this approach is the division of the search process into two stages and the application of different methods on each of them. At the first search stage it is used a genetic algorithm. At the second search stage an annealing simulation algorithm is proposed, which allows to improve the result found by the genetic algorithm. Based on this approach, a combined algorithm has been developed. A computational experiment was carried out on test examples (benchmarks). The quality of the obtained placement is on average 3.5% higher than the placement results obtained by using the well-known Dragon 2.23 algorithm. Series of tests and experiments were carried out and showed the promise of this approach. Time complexity of the developed algorithm is represented as  $O(n^3)$ .

**Keyword**— VLSI placement, annealing simulation, genetic algorithm, combined approach.

## I. INTRODUCTION

Modern human development in terms of scientific and technological progress in not assumes without automated and semi-automated manage systems of different processes and objects. During manufacture of new electronic equipment, great importance has computer aided design methods, which allow to create high-reliable very-large-scale integration circuits (VLSI) in a short term and at relatively low cost. The tendency to increase the VLSI integration degree leads to a significant increase in labor intensity in their design, that connection with the growth of problems dimensionality.

Among the design problems the VLSI placement is the most problematic stage since it is necessary to process large data sets. Currently, with the development of information technology, classical algorithms cannot solve this problem, because the placement problem is time consuming and researches are developed new heuristic, combined and hybrid approach for its solution [1-4]. So, the discussed problem is actual and important. The main aim of the authors is development and research of combined placement algorithm based on simulation annealing and genetic algorithms (GA).

## II. PROBLEMS OF VLSI DESIGN

Today, due to appearance of new technologies and transition to submicron devices, the placement problem has important value.

Generally, design is considered as transformation of technical design specification to the information necessary for its manufacture.

The result of the design is the release of project documentation.

Here, the following design methods are used: layout; physical modeling; calculation of analytical expressions; mathematical modeling and topology construction [4, 5].

One of the most important steps to simplify of the VLSI topology design process and taking into account new design standards Mead and Conway developed the following rules [6]:

- minimum width of conductors;
- minimum distance between conductors;
- energy preservation of a crystal;
- minimal signal delay.

During VLSI topology design, it is taken into account that each pin includes several layers, and rules applied to the conductors on these layers are also applied to contacts. Note, components arrangement within layers causes dynamical characteristics of VLSI. Due to the increasing of VLSI integration degree, labor intense is growth on this step. It should also be noted that the stronger the interrelation of the design stages, the higher the technical requirements for VLSI design. At present, the role of iterative design with adaptation properties sharply increases and takes place the integration of design stages.

During VLSI topology design, the following tasks must be solved: topology control; photomasks design; synthesis of topology [4].

The main tasks of the topology synthesis are: placement of elements on a crystal; connections between elements pins; partitioning of circuit into parts; library of elements and typical IP-blocks. Control of topology implies the solution of such problems as: verification and isomorphism.

The topology of library elements is predesigned, where the main criterion is the topology area of the circuit on the crystal with many restrictions. After the topology is constructed, the

verification stage is performed with the original switching scheme.

At each stage, the designer performs the same design procedures: structural synthesis, compilation of a mathematical model, analysis of a mathematical model, optimization of mathematical model parameters and its statistical analysis.

### III. PROBLEM FORMULATION

For VLSI placement problem the initial information are [5]:

- connecting field;
- connecting circuit with predetermined number of blocks;
- number of nets.

The model of the connected circuit contains the same type cells combined into lines. A typical cell is geometrical square unit with determined internal topology and known places for external connection. In our case, pins can be situated from either side.

Let us formulate the placement problem in the following way. On the suggested connecting field, it is necessary to place a set of elements with respect to each other in such a way that the system performance tends to be optimal. So, it is necessary to minimize the total length of the interconnections [2, 4].

Let us give a formal description of the VLSI placement problem. Let  $B_1, \dots, B_n$  are placed elements within connection field. Each element  $B_i | 1 \leq i \leq n$  is defined by geometrical dimensions: height  $h_i$  and width  $w_i$ . Let  $N = \{N_i | i = 1, m\}$  in a netlist and  $L_i$  is a length of net  $N_i | i = 1, m$ . So, the placement problem consists of finding rectangular areas within connection fields for each element from  $B$  and  $Q$ , and defined by a set of areas  $R = \{R_i | i = 1, n\}$  such that [6]:

- Each block is placed in corresponding rectangular area  $R_i$  with height  $h_i$  and width  $w_i$ .
- Areas from  $R$  do not intersect.
- Total area of described rectangular of set  $R$  tend to minimum.
- Total length of interconnections is minimized on the following way

$$F = \sum_{i=1}^m L_i, F \rightarrow \min$$

In the paper to find  $L_i$  - the length of  $i$ -th net the authors proposed to use combined algorithm.

### IV. ARCHITECTURE OF COMBINED SEARCH METHOD

Recent research in CAD shows that due to the processing of big data it is necessary to use heuristic combined and hybrid approaches, based on prior knowledge about tasks being solved. So, the authors proposed to use the combined strategy "Evolution-Search" presented in Fig. 1. To implement this strategy in the Block "Evolution", genetic search methods are used, and in the Block "Search" - the annealing simulation algorithm [8, 9].

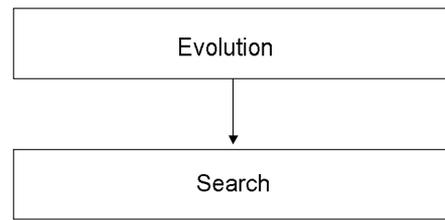


Fig. 1. Search strategy "Evolution-Search"

To implement this strategy, it is used a combined search architecture based on a combination of a genetic algorithm and an annealing modeling algorithm (Fig. 2).

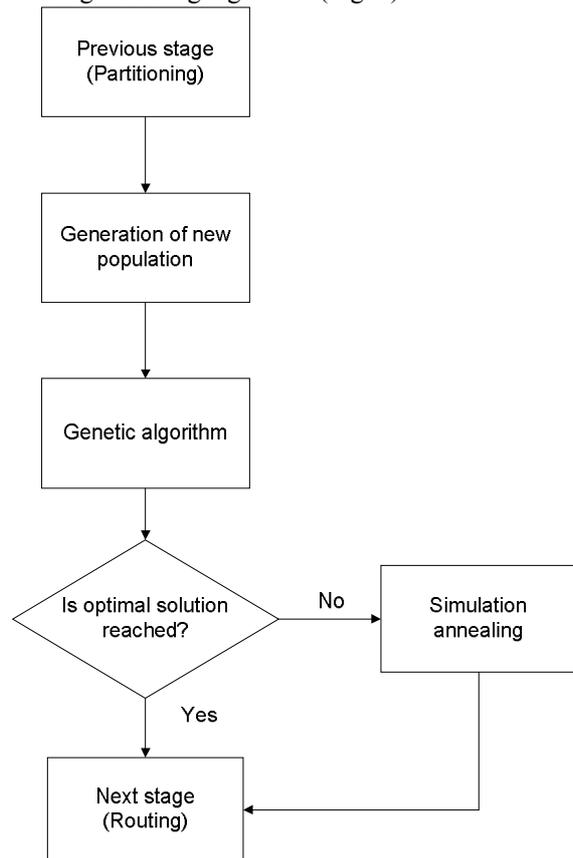


Fig. 2. Architecture of combined search method

Input data, here, are data from the previous stage of design – partitioning. Next, there are generate a population of initial solutions.

It is necessary to obtain from the random VLSI fragments placement an order with a minimum value of the objective function.

The next step is the implementation of the genetic search. In the genetic algorithm, new solutions are generate on the basis of various modified genetic operators, such as crossing-over, mutation, reduction, etc. [9, 10].

Then, it is necessary to check whether the optimal solution was found. If this solution is optimal, from the point of view of the objective function value, the algorithm is terminated

and transfers the results to the next design stage - routing. If the optimal solution is not found, as a result of the GA, the best solution from the set is chosen and transferred to the annealing modeling algorithm for its improvement [8]. Such search strategy has the following advantages: it allows to obtain optimal and quasi-optimal solutions in polynomial time; consider more promising ones and remove unpromising decisions and does not require knowledge about providing additional information, which indicates the effectiveness of the suggested approach.

**V. SCHEME OF THE COMBINED ALGORITHM**

The VLSI fragments placement contains the following stages: generation of initial solutions; forming of initial population; the first search stage based on GA and results improvement based simulation annealing method.

Based on the suggested strategy and the presented architecture, there is developed a combined algorithm presented on Fig. 3 [11, 12].

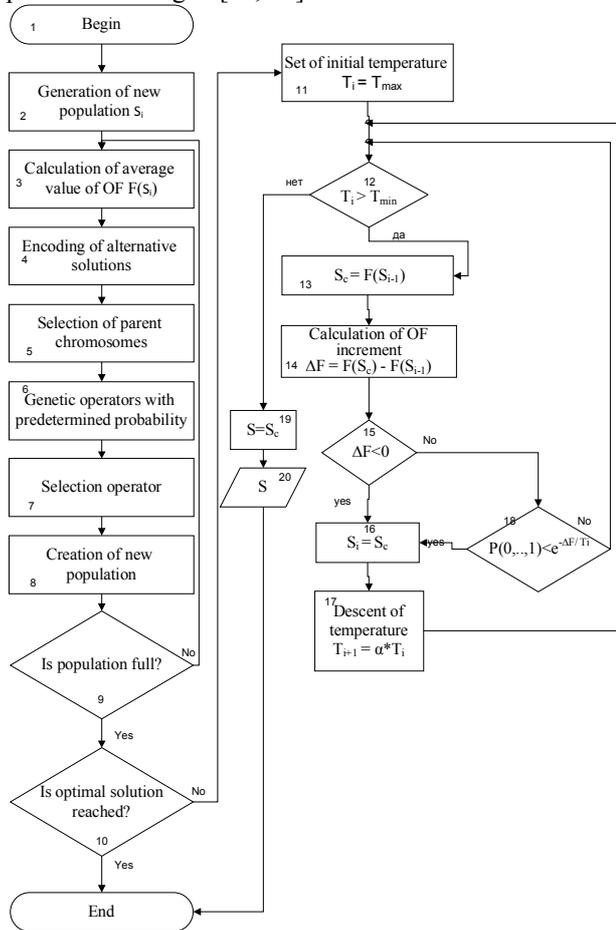


Fig. 3. Scheme of combined algorithm

The algorithm begins its work with the generation of the initial population. Then, the average value of the objective function is calculated. For implementation of genetic operators (crossover, mutation, inversion) with predetermined probability there are selected parent chromosomes. The

number of alternative placements is determined to exclude them from the population, so that its size remains constant. Verification of the stopping criterion achievement is a finding of the optimal solution. If the optimal solution is found, then the algorithm finishes its work. Otherwise, the annealing simulation algorithm is started. Its work continues until the stop criterion is reached - the minimum temperature.

Note, that the proposed approach makes it possible to obtain optimal or quasi-optimal solutions in polynomial time. The time complexity of this algorithm lies in the range of  $\sim O(n^3)$ .

**VI. EXPERIMENTS**

To carry out the computational experiment, a software environment was developed that implements the developed combined algorithm for the VLSI fragments placement. A series of experiments was performed for a different set of test cases, differing in the number of elements in the circuit. The averaged results of the experiments are shown in Fig. 4. Time complexity is represented as  $O(n^3)$ , which confirmed the theoretical and practical significance of the developed algorithm for solving the problem of VLSI fragments placement.

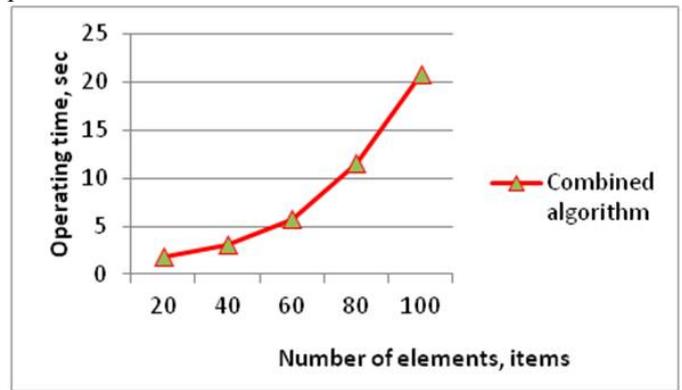


Fig. 4. Dependence of the developed algorithms' operating time on the number of the circuit elements

To estimate the effectiveness of the suggested approach, a computational experiment was performed on a set of test cases [12, 13]. For comparison, there are selected the following algorithms: Dragon 2.23, iterative and developed combined algorithm. Fig. 5 shown comparison of quality of solutions obtained by given algorithm.

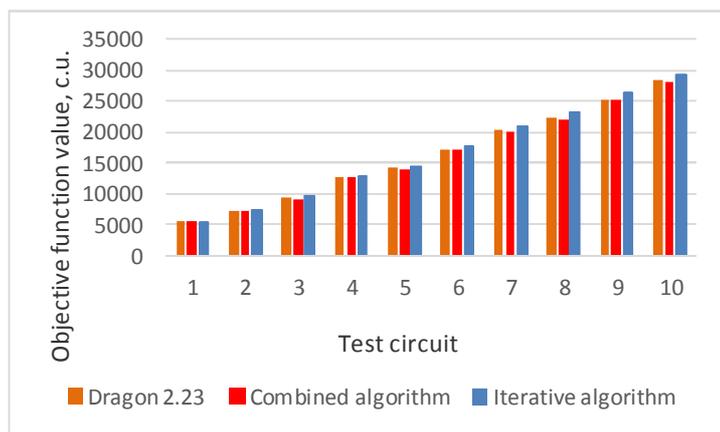


Fig. 5. Comparison of the solutions quality obtained by the developed combined algorithm.

Based on the analysis of the conducted studies, the quality of placements obtained by the combined approach is 3.5% higher than the placement obtained by the Dragon 2.23 algorithm and the iterative algorithm. That indicates the effectiveness of the developed approach.

### VII. CONCLUSION

In this paper, the authors suggested a strategy of combined search "Evolution - Search". The combined search architecture based on a combination of genetic search and an annealing modeling algorithm has constructed. To implement this strategy, the VLSI placement combined algorithm has been developed, which makes it possible to reduce the number of computational resources and the time for searching optimal and quasi-optimal solutions.

To determine the effectiveness of the proposed approach, a software product was developed. A computational experiment was performed, which allowed to confirm theoretical estimates of the speed and efficiency of the developed combined algorithm. A comparison with the Dragon 2.23 algorithm and the iterative algorithm was carried out.

The time complexity of the developed algorithm is represented as  $O(n^2)$ .

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### REFERENCES

- [1] J.P.Cohoon, J.Karro, J.Lienig, "Evolutionary Algorithms for the Physical Design of VLSI Circuits. Advances in Evolutionary Computing: Theory and Applications", Ghosh, A., Tsutsui, S. (eds.) Springer Verlag, London, pp. 683-712 (2003)
- [2] G.F.Luger, "Artificial Intelligence. Structures and Strategies for Complex Problem Solving", 6th Ed. Addison Wesley, Boston MA (2009)
- [3] Kureichik, V., Jr., Kureichik, V., Bova, V. Placement of VLSI fragments based on a multilayered approach (2016) Advances in Intelligent Systems and Computing, 464, pp. 181-190.
- [4] C. J.Alpert, P.M. Dinesh, S.S.Sachin, "Handbook of Algorithms for Physical design Automation", Auerbach Publications Taylor & Francis Group, USA (2009)
- [5] V.V.Kureichik, D.V. Zaruba, "The bioinspired algorithm of electronic computing equipment schemes elements placement". In: 4th Computer Science On-line Conference, CSOC 20156 Silhavy. R., Senkerik. R., Oplatkova. Z. K., Prokopova. Z., Silhavy, P. (Eds.), vol. 347, pp. 51-58, Springer Verlag (2015)
- [6] D.Y. Zaporozhets, D. Zaruba, V. Kureichik, "Hybrid bionic algorithms for solving problems of parametric optimization", J. World Applied Sciences, vol. 23, pp. 1032-1036 (2013)
- [7] D.Y. Zaporozhets, D.V. Zaruba, V.V. Kureichik, "Representation of solutions in genetic VLSI placement algorithms", In: Proceedings of IEEE East-West Design & Test Symposium – (EWDTS'2014) Kiev, Ukraine, September 26 – 29, (2014)
- [8] Orlov, A., Glushchenko, A., Kureichik, V., Jr. Hybrid genetic algorithm for cutting stock and packaging problems (2016) Proceedings of 2016 IEEE East-West Design and Test Symposium, EWDTS 2016, art. no. 7807680
- [9] D. Zaporozhets, D. Zaruba, V.Kureichik, "Hierarchical approach for VLSI components placement", In: 4th Computer Science On-line Conference, CSOC 20156 Silhavy. R., Senkerik. R., Oplatkova. Z.K., Prokopova. Z., Silhavy. P. (Eds.), vol. 347, pp. 79-87, Springer Verlag (2015)
- [10] S.K. Lim, "Practical Problems in VLSI Physical Design Automation", Springer Science + Business Media B.V, Germany, (2008).
- [11] Zhao, H., Destech Publicat, I. VLSI placement design using genetic algorithms (2014) 2014 International Conference on Mechanical Engineering and Automation (ICMEA), pp. 436-439.
- [12] Wang M., Yang X., Sarrafzadeh M. Dragon2000: Standard-cell Placement Tool for Large Industry Circuits – ICCAD2000, pp. 260-263.
- [13] J. Kacprzyk, V.M. Kureichik, S.P. Malioukov, V.V. Kureichik, A.S. Malioukov, "Experimental investigation of algorithms developed. Studies in Computational Intelligence", 212, pp. 211-223+227-236 (2009)