TCAD simulation of MIS-gated power GaN transistors

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Abstract—E-mode AlGaN/GaN HEMTs are generally promising candidate for switching power transistors due to their high breakdown voltage, high current density and low on-resistance. The threshold voltage (Vth) of normally-off mode AlGaN/GaN HEMTs with a self-aligned p-type GaN gate can be successfully improved by inserting a SiN insulator between the p-GaN and a Schottky gate electrode. The Vth can be increased from +1.5 V to +6.8 V by inserting of 15 nm SiN layer. Moreover, the sub-threshold drain and on-state gate currents of p-gate GaN transistor were decreased.

Keywords—power electronics, GaN transistor, p-GaN, self-aligned, threshold voltage, Schottky, MIS-gate

I. INTRODUCTION

GaN based high electron mobility transistors (HEMTs) are excellent devices for application in power electronics. To realize high-efficiency and high-power inverters, low-on-resistance, high drain current and high breakdown voltage devices are needed. AlGaN/GaN high electron mobility transistors are very promising for realizing such efficient electron devices [1]. High-power devices should be operated in the normally off mode to realize a fail-safe system. However, most of the AlGaN/GaN HEMTs are operated in the normally on mode. Normally off p-type gate GaN HEMTs are promising for the realization of high power and low-loss switching devices because the leakage drain current is very low at zero gate-source bias [2]. To realize fail-safe operation, the threshold voltage of normally-off mode transistors should be higher than +2 V to prevent an incorrect action. Normally-off HEMTs based on metal-insulator-semiconductor (MIS) gate structure with full recess AlGaN have been already reported by several groups [3]-[8]. There is low gate leakage, threshold voltage higher than one volt. But the main drawbacks of this approach are the threshold voltage instability (positive [9], or negative [10]) due to the interface/border traps in the insulator, and the time dependent dielectric breakdown of the thin insulator [11] - [14].

In this study we present TCAD simulation and experimental results of MIS-gated power GaN transistors to increase the threshold voltage and reduce gate leakage of e-mode power switching devices.

II. EXPERIMENTAL

The p-GaN/AlGaN/GaN epitaxial structures produces by MOCVD on silicon substrates were used in experiments. The structures include the GaN:Fe doped buffer layer (2 um), i-GaN channel, Al0.25Ga0.75N barrier layer (10 nm) and Mg-doped p-GaN layer (60 nm) with Mg concentration of 5x10^19 cm^-3. The SiN layer (gate insulator) with thickness form 0 to 15 nm was deposited by PECVD on full wafers. Then Pd gates were directly e-beam evaporated on SiN layer. After that SiN was etched away by RIE using Pd metal as hard mask. p-GaN layer was selective etched in BCl3/SF6 to form the self-aligned MIS-gate structure. After the formation of device isolation area, the low temperature (550 °C) Ta/Al based ohmic contacts are e-beam evaporated followed by 170 nm PECVD SiN. The device size is a gate length of 1 um, a gate width of 100 um and a gate-drain distance of 6 um. The source-gate separation is 1 um.

The DC parameters of the fabricated GaN transistors were measured by HP4156A Semiconductor Parameter Analyser.

Fig. 1 shows a schematic view of the fabricated self-aligned MIS-gated GaN device structure.
III. RESULTS

Fig. 2 shows a band diagram of gate area. The double heterojunction is formed in p-GaN gate region between p-GaN/AlGaN and AlGaN/GaN.

Fig. 3 shows the $I_{ds}$-$V_{gs}$ DC characteristics of fabricated AlGaN/GaN HEMTs. It can be seen that the Pd Schottky gated (SiN: 0 nm) GaN transistor has $V_{th} = +1.5$ V and sub-threshold drain leakage current at $V_{gs} = 0$ V is 3 µA/mm. The maximum drain current is $I_{ds} = 0.52$ A/mm at $V_{gs} = 15$ V. The threshold voltage of MIS-gated HEMTs with SiN thickness of 5, 10, 15 nm is about 1.7 V, 3.8 V, 6.8 V, respectively. It is visible from Fig. 3 that increase of SiN thickness in MIS-gate structure lead to reduce the magnitude of sub-threshold drain leakage current. It can be caused by the reduced trap density at the SiN/p-GaN interface after PECVD passivation. However MIS-gated GaN transistors with thick (15 nm) insulator demonstrate the reduced maximum drain current $I_{ds} = 0.25$ A/mm at $V_{gs} = 15$ V.

Fig. 4 shows $I_{gs}$-$V_{gs}$ characteristics. It can be seen that the fabricated p-gate GaN HEMT with Pd based Schottky contact has the high on-state gate current. The maximum gate swing is about $V_{gsmax} = 5 – 6$ V. Introduce the thin SiN layer (5 nm) between Schottky metal and p-GaN layer lead to significantly reduce the on-state gate current and increase the gate swing to $V_{gsmax} = 12 - 15$ V. Further increase the SiN thickness lead to reduce on-state gate current. The fabricated self-aligned MIS-gates GaN HEMT with 15 nm SiN insulator demonstrates the low on-state gate current $I_{gs} = 0.1$ µA/mm at $V_{gs} = 15$ V.

Fig. 5 shows the dependences of threshold voltage and maximum drain current from the SiN thickness (0, 5, 10, 15 nm) in MIS-gates GaN AlGaN/GaN HEMTs. Increase the SiN thickness from 0 to 15 nm lead to improve the threshold voltage value from 1.5 V to 6.8 V. There is visible a linear decreasing of maximum drain current from the SiN thickness in MIS-gate structure.
The p-doped GaN layer on top of the AlGaN barrier and the GaN channel form a pin-diode, this diode gradually started turning on upon increasing positive gate bias. The top Schottky type gate contact is in reverse polarity with respect to the semiconductor-junction pin-diode.

Fig. 5. Dependences of threshold voltage and maximum drain current from the SiN thickness in MIS-gated AlGaN/GaN HEMT.

Fig. 6 shows the equivalent circuits of (a) Schottky and (b) MIS-gated GaN HEMTs. The drain current is turned on when the gate voltage supplies to AlGaN capacitance ($C_{\text{AlGaN}}$) becomes higher than the threshold voltage ($V_{th}$), because the circuits are connected to gate AlGaN by two dimension electron gas (2DEG) when the threshold voltage is applied. The $V_{th}$ changes with the series capacitance when the gate insulator is inserted. The relationship between the $V_{th}$ and total capacitance of MIS-gated HEMTs is shown in formula (1), in which $V_{th}(\text{Schottky})$ is the $V_{th}$ of Schottky contact HEMTs, $V_{th}(\text{MIS})$ is the $V_{th}$ of MIS-gated HEMT and $C_{\text{ins}}$ is the insulator capacitance.

$$C_{\text{AlGaN}} \cdot V_{th}(\text{Schottky}) = C_{\text{ins}} \cdot \left( V_{th}(\text{MIS}) - V_{th}(\text{Schottky}) \right)$$

$$V_{th}(\text{MIS}) = \frac{C_{\text{AlGaN}} \cdot V_{th}(\text{Schottky})}{C_{\text{ins}}}$$

(1)

Fig. 6. Equivalent circuits of Schottky and MIS-gates GaN HEMTs.

Fig. 7 shows the experimental results of SiN thickness and $V_{th}$. The broken line shows the results of TCAD simulation. The experimental results almost coincide with the results of simulation.

Fig. 7. Dependences of threshold voltage from SiN thickness of MIS-gated AlGaN/GaN HEMT from TCAD simulation and experimental results.
There known two different concepts to produce normally-off GaN devices: Schottky and Ohmic p-gate devices. Panasonic [15] – [16] and FBH [17] – [19] are used the Ohmic contact to p-GaN layer, but Samsung [20] and IMEC [21] are used the W and TiN based Schottky gate contacts. A detailed investigation of the impact of gate metal on the performance of p-GaN/AlGaN/GaN transistors was presented in [22]. The authors of this study demonstrated that the work function of the gate metal has a critical impact on the electrical parameters of the devices, such as off-state leakage, forward operation current and threshold voltage. Several gate metals (Ni/Au, Ti/Au and Mo/Ti/Au) were compared, to discuss the importance of the trade-off between $V_{th}$ and output drain current. According the data from Fig. 7, in this work Schottky based MIS-gated GaN transistors with different insulator layer thickness (5, 10, 15 nm) demonstrate the better $V_{th} – I_{ds}$ performance.

Moreover, using MIS-gate in p-GaN transistors is possible to obtain very low on-state gate current values up to a gate voltage of 15 V (fig. 4), which is preferred for reliability and for compatibility with gate drivers, that are often designed for insulated gate technologies and to lower the power consumption (i.e. high gate leakage is associated with a continuous power consumption and associated heating of the gate driver).

IV. CONCLUSIONS

High voltage enhanced mode GaN transistors is a basic element for power electronic applications. For achieving normally-off operation p-type GaN gate structures are used. The optimized epitaxial designs enable threshold voltage close to $+2$ V. In present work, it was shown that SiN gate insulator introduced into p-GaN gate HEMT lead to increase the threshold voltage up to $+6.8$ V. The threshold voltage can be controlled by changing the thickness of SiN layer. The subthreshold and on-state gate currents were decreased. Therefore, DC power loss of the input signal was decreased.

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