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Multi-chip assembly based on SiP technology

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Abstract: System in package（ SIP） is characterized by any combination of more than one active electronic component of different functionality plus optionally passives and other devices assembled preferred into a single standard package that provides multiple functions associated with a system .this paper introduces the classification and superiority of SIP encapsulation through the research and development of system encapsulation technology, and discusses the simulation and application of Multi - chip SiP package.

1. Introduction

In recent years, electronic packaging from the original supporting role promoted to the current key role, with the rapid development of the semiconductor industry and its rapid penetration to other industries, as the connection between electronic systems and semiconductor chips, the importance of electronic packaging to be more reflected.

The main stages of the development of electronic packaging technology as shown in Figure 1:

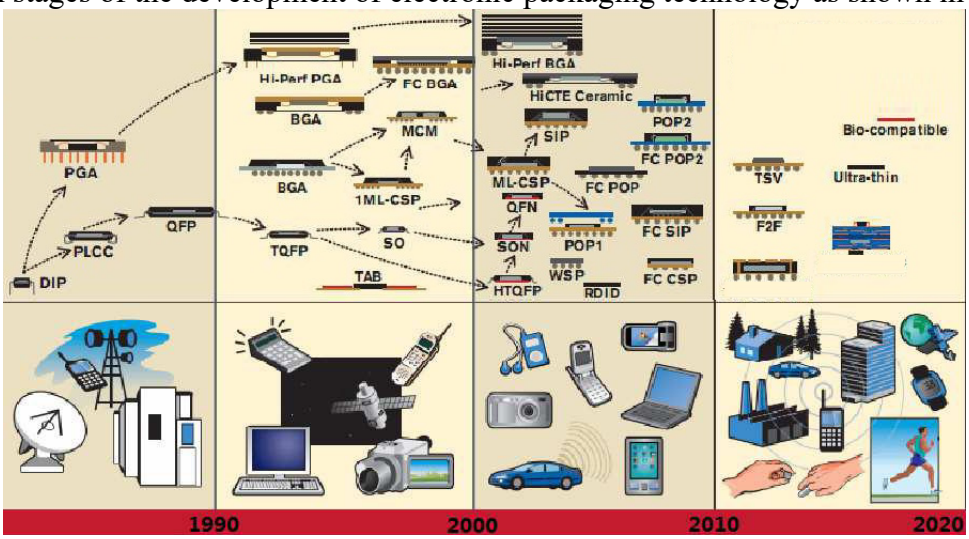

Figure 1 The development trend of electronic packaging technology

System-level package technology is a high-density integration technology that integrates multiple dice and peripheral devices in a single package and performs certain system functions. The die can be stacked, tiled, and embedded in the substrate. The peripheral devices are embedded in the substrate and the surface mounting technology in the form of thin film. The electronic system is miniaturized, high performance, multi-function, high reliability and low cost.

For the purpose of system integration, the world's major systems integration technology line contains three:(1) System-on-Chip(SoC); (2) Multi-Chip-Module(MCM); (3) System-in-Package(SiP).

2. SIP Technology

2.1. The Advantages of SIP Technology

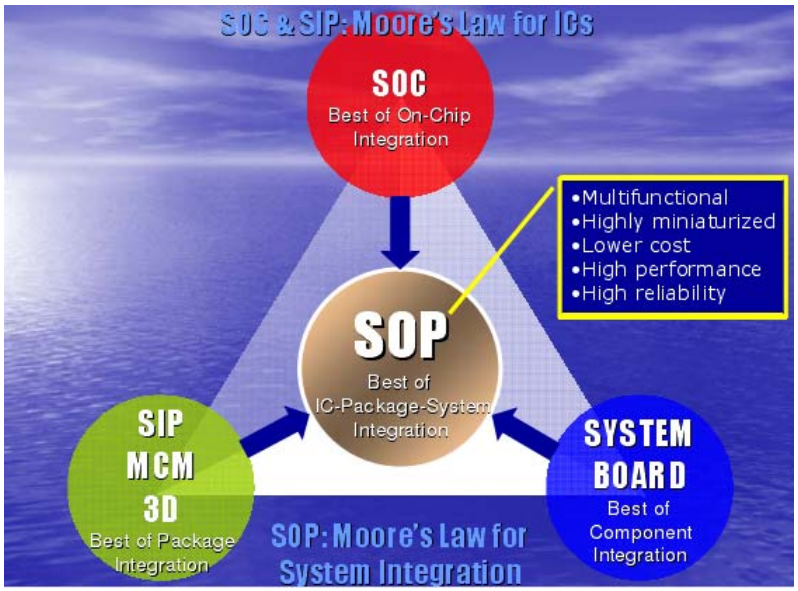

Figure 2 High density integration of electronic systems

SoC integration technology is a lot of functional modules integrated in a single semiconductor chip. For example, a microprocessor, a memory, an input / output controller, or a high-frequency wireless transceiver module, a digital processing module, etc., are integrated on a silicon wafer to complete the miniaturization of the system. But the system chip integration technology in the integration of passive components will be from the design, materials to the process of serious restrictions, thus affecting the system function, it is difficult to complete the real system integration. From another perspective, the system chip integration technology has been proposed for more than 40 years, but so far the development of slow, much lower than the original expectations. The reason is that there are many aspects, mainly the system chip integration involves the interface of each module, the mutual influence of each module, as well as the module of intellectual property and other issues. This is a very complicated system engineering. System chip integration process in a variety of semiconductor materials is difficult to compatibility between. In addition, if the definition of the larger the system, the higher the difficulty of design. The larger the area of the semiconductor, the lower the yield. Large areas can also lead to increased signal transmission delay, increased attenuation and other negative effects. Experts who are engaged in system-on-chip integration also acknowledge that chip system integration is far more difficult than expected.

MCM packaging technology is a number of different functions of the semiconductor die tiled or overlapping installed on a substrate, and then packaged up. As the multi-chip package of the substrate is only to play the role of these die together, and no other features, so multi-chip packaging technology can only be a subsystem and not a real sense of the system integration technology.

SIP is the real sense of the system integration, because it contains all the components of an electronic system.it is a different function of the die in a flat or overlapping way, the surface mount or embedded in the substrate, while the as many passive components embedded in the substrate and the substrate functional, the surface only install the active components and May be less passive components..

2.2. Advantages of SiP Relative to Board-Level Circuits

SiP technology can shorten the distance of the metal connection, and thus its parasitic impedance (resistance / capacitance / inductance) to reduce the transmission speed, electromagnetic interference is improved, power consumption is also greatly reduced, so the chip performance good. More importantly, the reliability of the system is greatly improved by integrating the functional

components or passive components in a package with less interconnection for the following reasons: (1) the number of components assembled on the surface, the number of solder joints and (2) because of the complex multi-layer cavity three-dimensional structure and the conductive hole grounding "wall" of the formation of a strong isolation capacity, making a variety of different signals may be in the same package (3) in a package contains a number of circuits and independent packaging of the module compared to the required number of shell, the number of external walls, the volume of the outer wall, the number of external walls, And the number of components are greatly reduced, which means that the packaging manufacturing and assembly required less labor time, and thus the lower the cost.

2.3. Classification of SiP

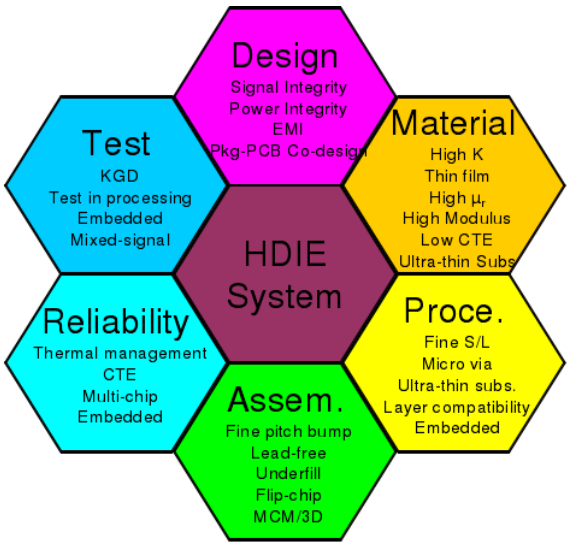

Figure 3 SiP technology research

From the current industry SiP design type and structure distinction, SiP can be divided into three categories:

(1)2D SiP: This package is in the same package on the substrate will be a one by one arrangement in a two-dimensional mode package in a package body;

(2)Stacked SiP: This package is a physical method in a package will be two or more chip stack integration up to package ;

(3)3D SiP: This package is based on the 2D package, and even the wafer stacking interconnection, constitute a three-dimensional package, the multi-chip chip, package chip, multi-chip group This structure is also known as laminated 3D package.

3. Multi-chip SiP Package

With the development of the chip packaging process, the number of packaged chip stacks is increasing, while the miniaturization of the package requires encapsulationOf the total thickness of the change is not large, which makes the new process can be very good to adapt to the original equipment, but it also means that the stack of each layer of the chip thickness must be reduced.

In order to ensure that the existing process is not a wide range of changes, usually by thinning the thickness of the chip to ensure that change the total thickness of the multi-chip SiP package, in the heat treatment process, reducing the thickness of the chip will increase the bending of the chip change, resulting in increased stress between the chip, when the stress increases to a certain extent will damage the chip, such phenomena in the SiP packages are often reported. We know that the plastic seal can prevent the intrusion of water vapor into the plastic seal interface and the chipreducing the thickness of the sealant, its ability in this area is bound to be weakened, so that it will have a crack and its expansion
to promote the role of it. For multi-layer chip SiP package devices, the introduction of patch and wire and other new technology, will greatly affect its reliability. At present, a great deal of research

has been done on the reliability and failure mechanism of single-chip packaging devices.the existence of the failure mode has a more comprehensive understanding, mainly: the thermal fatigue of the solder ball, chip and patch between the points layer, device thermal stress and moisture caused by failure. And the reliability and failure analysis of double chip chip SlP package of the reported less, for example: through the bending test to analyze the reliability of the package, with the finite element method to analyze the chip patch a high degree of impact, reliability of solder joints, etc., especially with respect to failures caused by structures and processes.

For the ultra-thin multi-chip SiP packaging process challenges, the general use of finite element software Abaqus analysis of many factors on the ultra-thin multi-chip SiP package reliability.

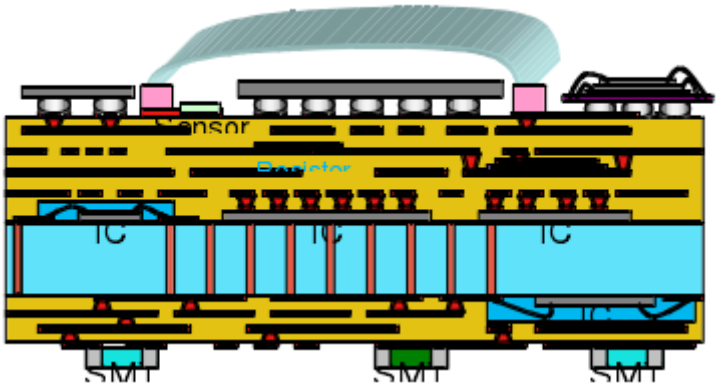

Figure 4 High density SiP package cross section

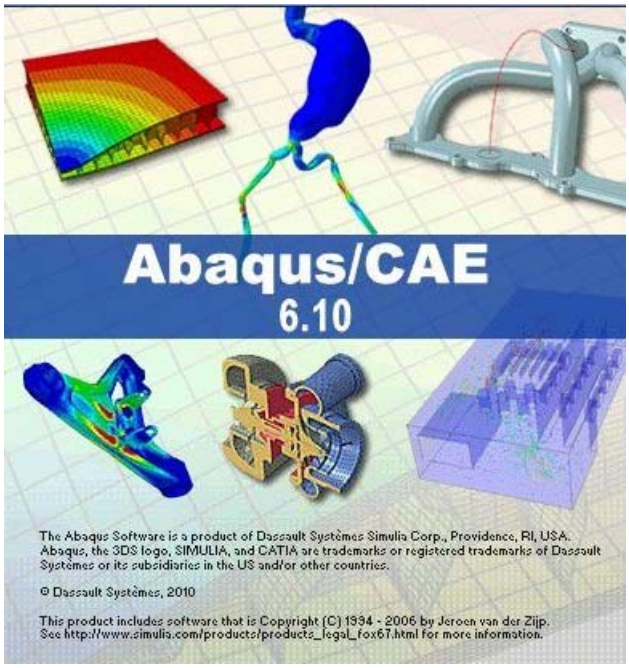

Figure 5 Abaqus finite element numerical analysis software

Through the use of Abaqus finite element numerical analysis software, the finite element model of the multi-chip SiP package, including the substrate, multi-layer adhesive layer, components and plastic materials, was established. The simulation results show that the encapsulated body Stress, strain, and possible failure forms. Compared with the same thermal load, the material properties of the plasticizer, the adhesive layer, the thickness of the chip and the adhesive layer were changed, and the stress and strain of the package were changed.

The optimization of the product design can be done by :

(1) finite element analysis of its structure, such as: Optimizing the design of the solder joint The dimensions are accurate enough to find potential design flaws and optimal, which will greatly reduce the stress concentration at the solder joint, And manufacturing costs significantly reduced.

(2) Through the finite element method to simulate the product in the production and use of the process of a variety of failure problems,Quantitative results, combined with experimental methods can quickly analyze the mechanism of failure.

(3) Thermal cycling failure of package, crack and layered prediction of package, thermal fatigue of device solder ball and solder joint can be used to simulate the finite element analysis.

Through the Abaqus simulation SiP package device failure mechanism and improved method, can be different failure modes and different processes on the device reliability.

4. Conclusion

This paper introduces the classification and superiority of SIP encapsulation through the research and development of system encapsulation technology, and discusses the simulation and application of Multi - chip SiP package.

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