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# Design of 4GHz CMOS Charge-pump Phased-locked Loop based on the Simulink Behavioral Simulation

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***Abstract*—According to the basic working principle and the structure analysis of the phase-locked loop, the simulation and analysis of the loop stability with the change of the main loop parameters have been finished according to the established third order dynamic model on the Simulink of the MATLAB, a fast transient simulation method and circuit design theoretical guidance of the charge pump phase-locked loop are provide in the paper. The 4GHz Charge pump phase-locked loop is implemented in the 0.18μm mixed-signal and RF 1P6M CMOS technology of SMIC.The chip area is 0.675 mm×0.700 mm. Based on the design and optimization of the loop parameters, the measured frequency of the VCO is from 3.98GHz to 4.3 GHz when the control voltage is chang from 0.3V to 1.5V, the measured phase noise of the CPLL is -91dBc/Hz at 100 kHz offset and -117 dBc/Hz at 1 MHz offset from the carrier 4.154 GHz under the locked stade.**

***Keywords-component; Phase-locked loop; Charge pump; Loop parameters; Phase noise***

## I. INTRODUCTION

In the wireless communication system, the phase-locked loop frequency synthesizer provides the receiver frequency conversion of the local oscillator signal in the RF receiver, and produce different center frequencies according to the channel planning,playing a very important role, with the vigorous development of the wireless communication technology. The phase-locked technology requirements are getting higher and higher. Now the current phase-locked loop chip towards the direction which has the advantages of high frequency, wide frequency band, high integration, low power consumption, low cost, powerful and so on. The charge pump phase-locked loop has the advantages of low power consumption, high speed, low jitter, static phase error approximately at zero, widely used in frequency synthesis, clock processing, etc., which has become the focus of the current phase-locked loop research[1-2]. In this paper,based on the analysis of the basic working principle and structure of phase-locked loop, the dynamic model of phase-locked loop is analyzed and simulated by MATLAB and Simulink, analyzing the relationship between the changes of the main loop parameters and the loop stability intuitively in the charge pump phase-locked loop, based on the analysis results, using the SMIC 0.18μm mixed signal and the RF 1P6M CMOS technology to complete the design of the 4GHz phase-locked loop.

## II. COMPONENTS OF THE CHARGE PUMP PHASE-LOCKED LOOP

Fig. 1 is a typical charge pump phase-locked loop (CPPLL) structure, making up of Phase Frequency Detector(PFD), Charge Pump(CP), Low-pass Filter(LPF), Voltage Control Oscillator(VCO) and Divider[3]. PFD does not require symmetrical pulses compared to the phase detector, and it can detect both the phase difference and the frequency difference, and the time required to convert from one frequency to another is greatly reduced. The outputs of the phase frequency detector and the charge pump are filtered by a low-pass filter to directly control the voltage-controlled oscillator.The divider in the feedback branch divides the output signal of the VCO which is compared with the reference signal ($f_{ref}$) through the phase frequency detector. In the integer frequency synthesizer, N is an integer[4].

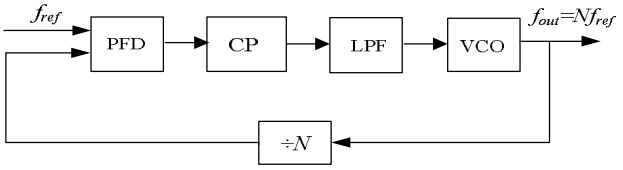


FIGURE I. TYPICAL CHARGE PUMP PHASE-LOCKED LOOP STRUCTURE

## III. BEHAVIORAL MODEL AND SIMULATION OF CPPLL

In the phase-locked loop design, the loop bandwidth is usually much smaller than the reference frequency. While the oscillation frequency of VCO in the large division ratio is the thousands of times of the reference frequency, transient simulation of phase-locked circuit level is a very slow process, needing to spend a lot of time and resources, so the behavior simulation which is based on the mathematical model has been widely used in the dynamic characteristics analysis of the PLL, which greatly speeds up the simulation speed[5].The common EDA design softwares are used to analyse the phase-locked loop dynamic characteristics, such as MATLAB with Simulink, VHDL-AMS, C language and ADS and so on,which provide the behavior simulation tools of the phase-locked loop dynamic model. But the method of MATLAB with Simulink is simple and easy to analyze the dynamic model of phase-locked loop. According to the charge pump phase-locked loop structure in Fig.1, the third-order CPPLL behavior model is established in Simulink as shown in Fig.2. Finally, complete content and

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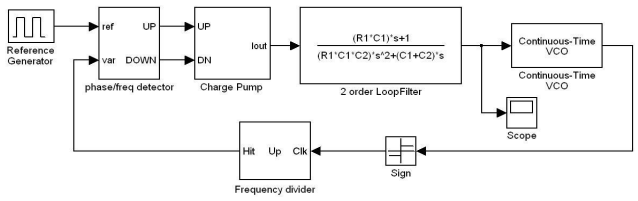


FIGURE II. BEHAVIOR MODEL OF CPPLL IN SIMULINK SIMULATION ENVIRONMENT

In Fig. 2, the low-pass filter uses a second-order passive filter structure, the capacitor $C_1$ connected in series with the resistor $R_1$, and then in parallel with the capacitor $C_2$.$C_1$ produces the first pole of the loop, the capacitor $C_2$ is used to reduce the ripple of the loop control voltage and produce the second pole[6-7]. In Fig.3, the basic loop parameters are the reference frequency $f_{ref}$, the charge pump current $I_{cp}$, the loop filter resistor $R_1$ and the capacitors $C_1$ and $C_2$, and divider frequency ratio N, VCO parameters mainly are free oscillation frequency $f_r$ and the gain coefficient $K_v$.

According to the structure of the second order passive filter, the transmission function of the loop filter which can be obtained is

$$F(s)=\left(R_1+\frac{1}{sC_1}\right)//\frac{1}{sC_2}=\frac{R_1C_1+1}{R_1C_1C_2s^2+(C_1+C_2)s}=\frac{1}{C_{total}}\frac{1+s/\omega_z}{s(1+s/\omega_{p2})} \quad (1)$$

where $C_{total}=C_1+C_2$, $\tau_1=R_1C_1=1/\omega_z$,

$$\tau_2=R_1\frac{C_1C_2}{C_1+C_2}=1/\omega_{p2}.$$

The open-loop transfer function of the third-order phase-locked loop is

$$H_o(s)=\frac{\theta_2(s)}{\theta_e(s)}=\frac{K_dK_v}{N}\frac{1}{C_{total}}\frac{1+s/\omega_z}{s^2(1+s/\omega_{p2})}=\frac{K}{R_1C_{total}}\frac{1+s/\omega_z}{s^2(1+s/\omega_{p2})} \quad (2)$$

where $K=(K_dK_VR_1/N)$, make $|H_o(j\omega_T)|=1$, the gain critical frequency $\omega_T$ of the loop which can be obtained is

$$\omega_T=K\cdot\frac{C_1}{C_1+C_2}\cdot\frac{\cos\phi_{p2}}{\sin\phi_z} \quad (3)$$

where

$\phi_z=\tan^{-1}(\omega_T/\omega_z)$, $\phi_{p2}=\tan^{-1}(\omega_T/\omega_{p2})$, the open-loop phase margin is

$$\varphi_m=\tan^{-1}(\frac{\omega_T}{\omega_z})-\tan^{-1}(\frac{\omega_T}{\omega_{p2}}) \quad (4)$$

The loop parameters of the third-order phase-locked loop are set as shown in Table 1, and the bode chart simulation of the open-loop transfer function is shown in Fig. 3. From Fig. 4 we can see that the amplitude curve has two turning points, respectively, at $\omega_z$ and $\omega_{p2}$. At low frequencies, the $1/s^2$ term plays a major role in amplitude, and the amplitude (gain) decreases with frequency, and the amplitude curve decreases at -40 dB / dec slope. At $\omega=\omega_z$ the zero point of the loop filter works, and the molecular term in the equation (2) makes the slope of the amplitude curve upward again at -20dB / dec. However,above the $\omega=\omega_{p2}$ , because of non-zero pole of the loop filter , the slope has become -40dB / dec. Since the initial amplitude slope is -40dB / dec, the asymptotic value of the phase curve begins to be -180º. Because of the zero point of the filter, the asymptotic value of the phase which is greater than the $\omega_z$ phase becomes -90º, and finally when the frequency is greater than $\omega_{p2}$, The near value becomes -180º again. Between the frequencies $\omega_z$ and $\omega_{p2}$, the phase curve appears a peak, so there is a local maximum at a particular frequency within this range. From the previous analysis we can obtain that the maximum value of the phase function is in $\sqrt{\omega_{p2}\omega_z}$ [8].

TABLE I. PHASE-LOCKED LOOP PARAMETERS

| $K_v$/MHz/V | $I_p$/mA | $f_{ref}$/MHz | $N$ | $f_T$/kHz | $\varphi$/° | $C_1$/pF | $C_2$/pF | $R_2$/kΩ |
|---|---|---|---|---|---|---|---|---|
| 160 | 1 | 4 | 1036 | 100 | 50 | 44.69 | 1414 | 4.20 |

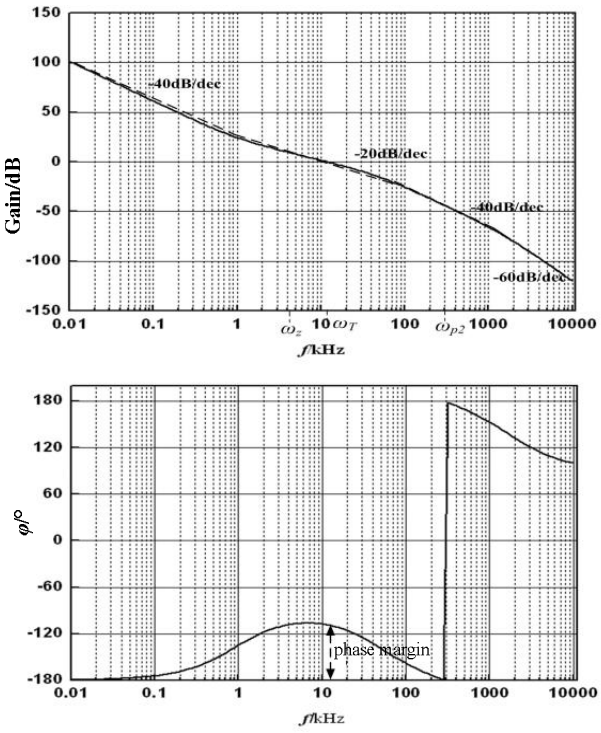


FIGURE III. BODE PLOT OF OPEN-LOOP TRANSFER FUNCTION FOR THIRD-ORDER PHASE-LOCKED LOOP

## IV. CIRCUIT DESIGN AND TESTING

The PFD design uses a falling edge-triggered digital frequency discriminator structure, as shown in Figure 4. The charge pump uses two pairs of differential inputs, so the structure uses the transfer gate and the inverter to generate two pairs of differential signals and reduce the phase dead zone by increasing the inverter delay unit on the reset signal path to reduce the accumulation of the VCO output phase noise. This phase frequency detector structure has a consistent phase difference conversion characteristic in the range of ± 360° and it is not sensitive to signal duty cycle.

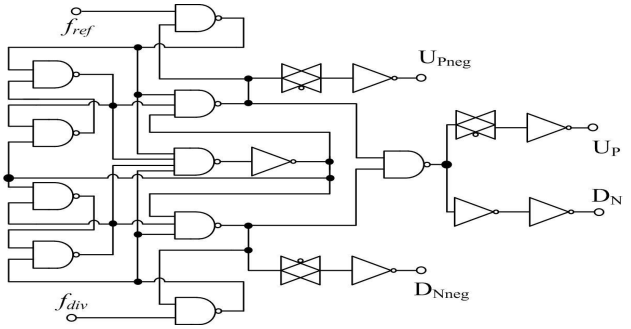


FIGURE IV. PFD CIRCUIT DIAGRAM

The charge pump uses the differential structure as shown in Fig. 5, and we introduce the unity gain amplifier to keep the common mode level of the two branches the same, avoiding the charge sharing problem.

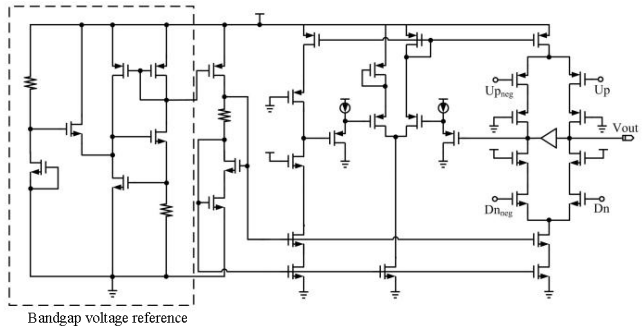


FIGURE V. DIFFERENTIAL CP STRUCTURE

VCO design uses the circuit structure shown in Fig. 6,making by the LC frequency tuning circuit and cross-coupling complementary differential pairs of tubes providing a negative feedback resistor;The complementary differential pair tube of the cross-coupling produces the negative resistance to counteract the loss of the LC resonant circuit.The LC frequency tuning circuit consists of slice-integrated planar spiral differential inductors, cumulative MOS variable capacity tubes and fixed high-Q MIM capacitors[9].The transistor can supply power between Mp1, Mp2 and Mn1, Mn2 mutually, so the tail current of VCO can be omitted, which can effectively eliminate the flicker noise of the circuit, and improve the output signal swing and improve the circuit performance. The planar spiral differential inductors L1 parameters are metal wire width 8μm, wire spacing 1.5μm, inductance inner diameter 30μm, turns 3,and the maximum Q value of the inductor near 4GHz is about 10, and the inductance is about 2.4nH. The variable capacitance range of the cumulative MOS variable capacity tubes $C_{v1}$ and $C_{v2}$ is 0.3 to 0.68pF, and the addition of the MIM capacitors $C_1$ and $C_2$ is in order to reduce the frequency adjustment range.

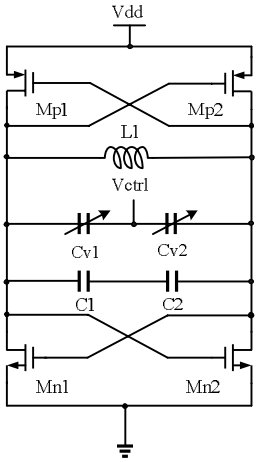


FIGURE VI. VCO CIRCUIT DIAGRAM

The programmable divider in the lower frequency division module utilizes VLSI design tool Apollo of the Synopsys to complete the layout of the circuit with CMOS standard cell library,and ultimately achieving with the SMIC 0.18μm mixed-signal CMOS technology.The total division ratio of the entire lower division module achieved is $N = K(PM + A)$, where K＝4，P=8，M＝32，A=3-10。Circuits use SMIC 0.18μm mixed signal and RF 1P6M CMOS process stream,and the chip photos made of are shown in Fig. 7. The chip area is 675μm × 700μm.

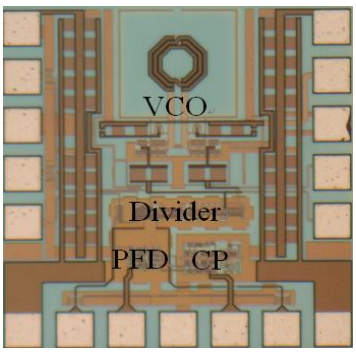


FIGURE VII. CHIP MICROGRAPH OF FREQUENCY SYNTHESIZER

According to the loop parameters of Simulink simulation optimization, the chip is tested for bonding test, and Fig. 9 is the VCO voltage control curve of the test, and VCO control voltages change from 0.3 to 1.5V, the oscillation frequencies are from 3.98 to 4.3GHz,Covering the design required frequency band. The divider frequency ratio is set to 1036, and the reference signal frequency is set to 4MHz.When the output signal frequency is equal to the reference signal frequency, the frequency synthesizer has entered the locked status. Fig. 8 shows the phase noise curve of the output signal that is

measured by the spectrum analyzer in the locked status (output frequency is 4.154 GHz). When the value of the deviation from the center frequency is greater than the loop bandwidth, and the phase synthesizer of the frequency synthesizer mainly comes from the noise of the internal voltage controlled oscillator. When the deviation frequency is within the loop bandwidth, the phase noise of the frequency synthesizer is mainly derived from the reference frequency source and the internal voltage controlled oscillator. The test results show that the phase noise is about -91dBc/Hz at 100kHz deviated from the center frequency, and the phase noise is about -117dBc / Hz at 1MHz deviated from the center frequency. When the entire frequency synthesizer supplies power under 1.8V supply, the consumption of the core current is about 13mA, where VCO core circuit is about 5mA, CP circuit about 3mA, the lower division and PFD about 5mA.

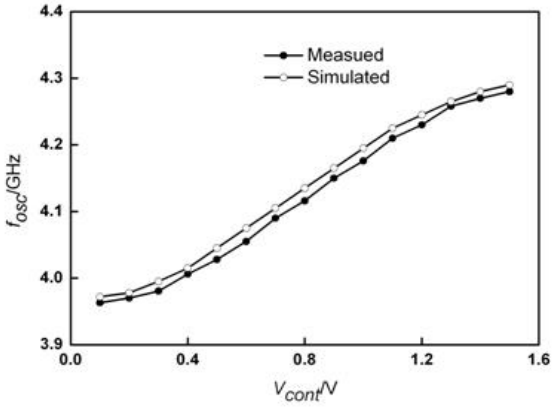


FIGURE VIII. VCO PRESSURE CONTROL CHARACTERISTIC CURVE

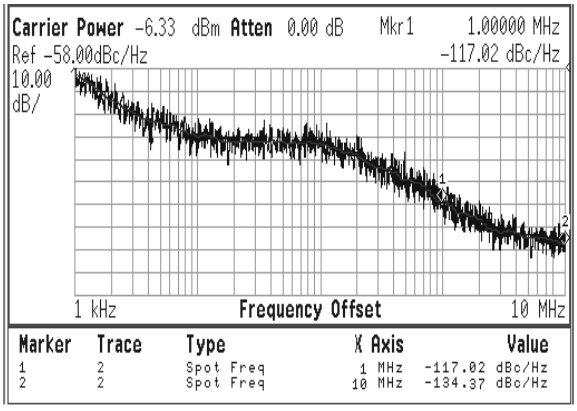


FIGURE IX. THE PHASE NOISE OF THE FREQUENCY SYNTHESIZER MEASURING WHEN LOCKED

## V. CONCLUSION

Based on the analysis of the basic working principle and structure of the PLL, the linear characteristics of the charge pump phase-locked loop circuit using the passive loop filter are researched, and the key parameters of the second-order charge pump phase-locked loop are deduced in detail. The dynamic model of the third-order charge pump phase-locked loop is established by MATLAB and Simulink. The parameters of the low-pass filter are optimized. The circuit is designed with SMIC 0.18 μ m mixed signal and RF 1P6M CMOS technology. The test performance is excellent.

## ACKNOWLEDGMENT

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