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Cascade H - Bridge Multilevel Inverter Based on Microcontroller

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***Abstract*—One of an H bridge Cascaded multilevel inverters was studied and designed. In this paper, the basic topology of microcontroller based H-bridge cascade multilevel inverter and the realization principle of control system are introduced. The principle and control strategy of the inverter are studied and described. Calculated by multi-superposition method, H bridge in the power field effect of the turn-off time is supposed to achieve the sine wave output, ladder wave modulation, with the switching device work in the fundamental frequency, small loss, and high efficiency. Circuit control part of the STM32 series chip by STMicroelectronics as the master chip, the device can run normally in the two H bridge out of the cascade of the state, causing a substantial increase in the reliability of the device; In EMTP power system in the electromagnetic transient analysis and simulation software,we construct a simulation model of 12H-bridge cascade. The simulation results show that the device can operate stably in the 12H bridge cascade state and n-1, n-2 state, which indicates the correctness and reliability of the design. In addition, the experimental device of 12H-bridge cascade multilevel inverter is designed, which realizes the design function and feasibility of this thesis.**

Keywords-H bridge cascade; microcontroller; multi-level inverter; redundancy; reliability operation;

I. INTRODUCTION

With the increasing demand for high voltage and high power conversion devices in industrial applications, multi-level inverter technology has attracted much attention from scholars both at home and abroad [1]. While withstand voltage of switching devices has been an obstruction of power conversion device voltage level to a further improvement, in order to use low-voltage switching devices to obtain multi-level high-voltage output, scholars have adopted: diode clamp multi-level structure, Flying capacitor clamp multi-level structure and H-bridge cascade multi-level structure [2]. Cascaded multi-level inverter has been widely studied and applied owing to its usage of low-voltages switching devices to achieve high voltage output.[3]. Although the first two methods has achieved a multi-level high-voltage output, there is voltage-sharing problem of DC capacitor partial pressure[4], and with the increase in the number of levels, the number of clamp diodes and capacitance increase significantly causing some difficulties with controlling and application of devices[5]. The H-bridge cascade multi-level structure, its basic power unit is cascade structure with an independent DC power supplied H-bridge and several H-bridge unit cascades, without DC capacitor partial pressure problem, while it has some advantages such as expanding more easily, outputting good quality voltage and with low harmonic content.

The existing H-bridge multi-level circuit in the practical application level exists the following problems [6]:

a) Low redundancy of structure, generally only meeting the demand of running the device in the n-1 state;

b) Higher cost of adopting IGBT;

c) Complicated power of control system and trigger system, demand of several sets of isolated power, as well as required by withstand voltage degree, tolerance value equals to voltage of access system;

d) Complex system information transmission wiring, in need of isolation, choosing optical fiber communications as communication forms, which costs much.

In this paper, an H-bridge cascade multilevel inverter is researched and designed under the premise of fully studying the current H-bridge cascade multilevel inverter. The main circuit part of the device adopts the cascaded H-bridge circuit, and the H-bridge triggering device adopts the crystal inverter for the gate-driven IGBT regulator or the gate-driven high-power MOSFET. The increase or decrease of the number of H-bridge cascade in this device can flexible control the output voltage, the main control adopting a STMicroelectronics STM32 series chip control two H-bridge circuit, making the chip function is fully utilized while reducing costs. In this paper, six groups of 12 bridge controlled by STM32 consist of multi-level inverter. The control algorithm uses multiple superposition method to calculate the turn-off time of each power field effect transistor, which makes the output voltage high-precision fitting sine wave output, and greatly reduces the harmonic problem of inverter voltage. The device is highly reliable, enabling full-state operation, n-1 and n-2 operation. Simulation and experiment verify the effectiveness of the device.

II. REALIZATION OF BASIC TOPOLOGY AND CONTROL SYSTEM OF H - BRIDGE CASCADE MULTILEVEL INVERTER

A. H Bridge Cascade Multilevel Inverter Basic Topology

In this paper, the design and implementation of STM32-based H-bridge cascade multi-level inverter device. The device consists of n H-bridge inverter unit, each H-bridge unit consists

of four full-control devices and an electrolytic capacitor, as shown in Figure 1. Each of the H-bridge units is equipped with an independent DC power supply, DC power supply with a three-terminal regulator device to achieve full-bridge rectifier.

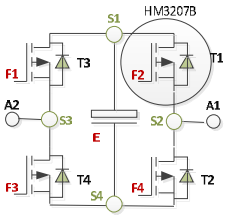


FIGURE I. H BRIDGE UNIT TOPOLOGY

B. *Realization of H - Bridge Cascade Multilevel Inverter Control System*

System structure shown in Figure 2. The circuit control part is powered by STMicroelectronics' STM32F103C8T6 with powerful control and signal processing capability. The chip has 32-bit ARM-based microcontrollers with 64KB bytes of flash memory, with two 12-bit modulo Converter, up to 16 input channels, while it has seven timers, nine communication interfaces. In order to realize the inverter work, the system has designed the following functions.

a) Trigger part

This design uses a chip to control the two H-bridge way, from a master chip issued a total of 8-way trigger signal for the No. 1 H bridge F1-F4, No. 2 H bridge F1-F4, 12H bridge cascade in this paper , A total of six master chip issued 48 trigger signal, the trigger signal to the optocoupler by a trigger pulse to achieve the gate to trigger the power field effect transistor. The trigger logic is described in detail by the following modulation strategy.

b) H bridge working state acquisition and monitoring part

The system acquires the voltage value on the bridge arm of the H bridge through the main controller to realize the working state acquisition and monitoring, and provides the reference quantity for the system to determine the operation mode. 1, the collection of S1, S2, S3 three-point voltage, through the low-power operational amplifier, the signal amplified to the main controller, the three signals that Figure 2, Q1, Q2, Q3.

c) Communication part

The system uses SPI (Serial Peripheral Interface) communication protocol, communication between the slave and the host computer. The slave machine to control the H bridge of each bridge voltage value passed to the host computer, the host computer according to the voltage value to determine whether the normal state of each H bridge, according to determine the number of work in the H bridge and each piece of STM32 chip Should control a group of H bridge number, the information back to the machine. The communication is a high-speed, full-duplex, synchronous communication bus, and occupies only four wires on the chip's pins, saving chip pins while saving space for PCB layouts, reliable and easy to use.

d) Trigger the power section

Trigger part of the power supply using magnetic ring transformer all the way to introduce three-step boost lead. After the use of full-bridge rectifier access three-terminal regulator circuit, the three-terminal regulator circuit after the photoelectric coupler to complete the trigger part of the power supply.

The main feature of this design is the STM32 and the main control system placed in a unified potential, and the trigger part of the power device and the power of the potential independent, so to solve the multi-level power supply needs more important issues, while meeting the STM32 power supply reliability, and communication using equipotential, eliminating the high cost of optical fiber communications.

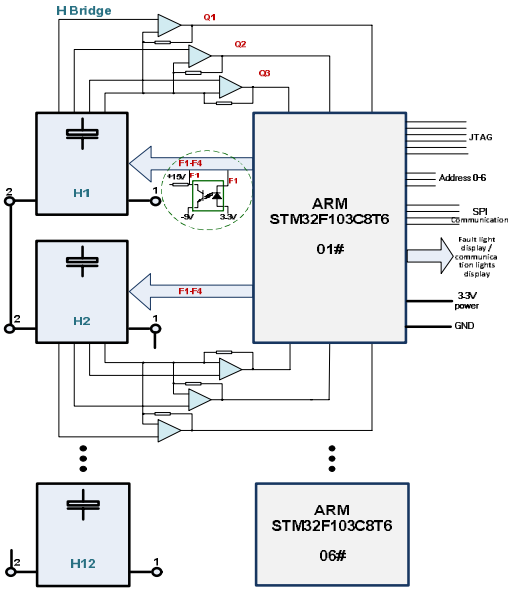


FIGURE II. STM32 - BASED H - BRIDGE CASCADE MULTILEVEL INVERTER TOPOLOGY

III. WORKING PRINCIPLE AND MODULATION STRATEGY OF H - BRIDGE MULTILEVEL INVERTER

A. *Principle of Single H - bridge in Continuous Conduction Mode*

Firstly, four working modes of single H-bridge circuit in H-bridge cascade multilevel inverter are analyzed. Figure 1, E is the electrolytic capacitor between the two plates voltage; T1-T4 for the four full-control devices, in this paper is used in a power field effect tube HM3207B, A1, A2 for the AC output.

(T1, T2, T3, T4), respectively, (1, 0, 0, 1), (1, 0, 1, 2, 4, (T1, or T2, T3, T4) = 1 means that T1 (or T2, T3, T4) turns on, (0, 1, 1, 0) , T1 (or T2, T3, T4) = 0 means T1 (or T2, T3, T4) turn off, because T1 and T2 and T3 and T4 at the same time will lead to short-circuit device, so the device chip to avoid triggering the same bridge Arm on the two power FET.

B. *H Bridge Cascade Multilevel Inverter Modulation Strategy*

The modulation strategy of the multi-level inverter determines the output performance of the inverter. This multi-level inverter uses multiple stacking method to realize the

function, which not only improves the output voltage waveform, but also improves the output voltage and power of the inverter and the number of transforms. When the switching device speed and rated power limit, only by the multi-level inverter itself can not achieve high-voltage high-power sine wave output, often also need to use multiple superposition method to expand and improve the output voltage waveform. In addition, in order to make the inverter better modular, hoping to use H bridge to achieve high voltage high power three-phase multi-level voltage output, it is necessary to achieve expansion, improve the output voltage waveform, but also phase transformation, In this case also use more from the superposition method to achieve. The sine wave modulation strategy of this inverter adopts the cosine law of multiple superposition method to calculate the turn-off time of four power field tubes on each H bridge accurately, and then fit the sine wave. In addition, the device innovation and reliability lies in, can work in the following three states:

a) All the H bridge in the equipment running state, this state for the device to run the whole state, the output voltage waveform is excellent, to achieve high-performance inverter function, with a stable working condition.

b) In the case of a H-bridge failure in the device, the STM32 microcontroller chip automatically identifies the fault bridge chain, then cuts it out of the cascade connection with the remaining H bridges, and then the micro-controller is enabled in an H-bridge fault condition Under the operating parameters, change the remaining bridge in the power of each power FET turn-off time, continue to fit the sine wave to protect the remaining H bridge to continue cascade operation, making the output voltage waveform is still good to meet the design requirements, Reliability.

Equipment in the case of two H bridge failure, then the device control core STM32 microcontroller chip is still automatically identify the device in the fault bridge chain, the fault bridge chain and the rest of the normal work H bridge cascade, while using two H bridge failure in the case of operating parameters, and assigned to the rest of each still running a normal bridge chain, change the power field effect of the turn-on time, continue to fit the sine wave to protect the inverter normal Work, this time the output voltage waveform is less than all H bridge cascade running state, but the output waveform still meet the design requirements and standards.

In particular, the modulation strategy is to divide the sine wave of one cycle into 2N relative time periods along the time axis. This time period is called the order width, and the sine wave voltage is integrated and divided $u = U_m \sin \omega t$ by Time period (step width), we can get the amplitude of each step of the ladder wave. Then sine wave voltage

$$u = U_m \sin \omega t \tag{1}$$

Is the fundamental component of the ladder wave.

The amplitude of each step of the ladder wave is expressed as follows

$$U_i = \frac{U_m}{\pi / N} \int_{(i-1)\frac{\pi}{N}}^{i\frac{\pi}{N}} \sin \omega t d(\omega t)$$

$$= \frac{2NU_m}{\pi} \sin \frac{\pi}{2N} \sin(2i-1)\frac{\pi}{2N}$$

$$i = 1,2,3,\cdots,2N \tag{2}$$

$$U_{i-1} = \frac{2NU_m}{\pi} \sin(2i-3)\frac{\pi}{2N} \tag{3}$$

So the order is

$$\Delta U_i = U_i - U_{i-1} = \frac{4NU_m}{\pi} \sin^2 \frac{\pi}{2N} \cos(i-1)\frac{\pi}{N} \tag{4}$$

In the formula, U_m is ladder wave amplitude,N is the number of cascaded H bridges.

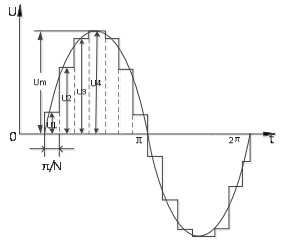


FIGURE III. CLOSE TO THE SINE OF THE MULTI-LEVEL LADDER WAVE

It can be seen from Fig. 3 that the amplitude of each square wave voltage is 1/2 of the corresponding order, respectively, so the amplitude of the square wave voltage synthesized by each H bridge is

$$U_i = \frac{2NU_m}{\pi} \sin^2 \frac{\pi}{2N} \cos(i-1)\frac{\pi}{N} \tag{5}$$

As can be seen from Fig. 4, the synthesized voltage step wave is an odd function, so there are only sinusoidal terms in its Fourier series.If used $f(\omega t)$ to represent the synthesized voltage step wave shown in Fig. 4, there is

$$f(\omega t) = \sum_{n=1,3,5,\cdots}^{\infty} U_{m(n)} \sin n(\omega t) \tag{6}$$

The coefficient of the sine term $U_{m(n)}$ is following formula:

$$U_{m(n)} = \frac{1}{\pi} \int_0^{2\pi} f(\omega t) \sin n(\omega t) d(\omega t) \tag{7}$$

Put the $f(\omega t) = U_i$ into the above formula and get it

$$U_{m(n)} = \frac{2NU_m}{2\pi^2}\sum_{i=1}^{2N}[\int_{(i-1)\frac{\pi}{N}}^{i\frac{\pi}{N}} \sin\omega t d(\omega t)\int_{(i-1)\frac{\pi}{N}}^{i\frac{\pi}{N}} \sin n(\omega t)d(\omega t)]$$

$$= \frac{NU_m}{\pi^2}\frac{1}{n}[\cos\frac{(n-1)\pi}{2N} - \cos\frac{(n+1)\pi}{2N}]\times$$

$$\sum_{i=1}^{2N}[\cos(2i-1)\frac{(n-1)\pi}{2N} - \cos(2i-1)\frac{(n+1)\pi}{2N}] \quad (8)$$

As the $\cos x$ is the real part of the e^{jx}, so the above formula available

$$U_{m(n)} = \frac{NU_m}{n\pi^2}[\cos\frac{(n-1)\pi}{2N} - \cos\frac{(n+1)\pi}{2N}]\times$$

$$\mathrm{Re}[e^{-\frac{(n-1)w}{2N}j}\sum_{i=0}^{2N-1}e^{\frac{(n-1)2\pi}{2N}ij} - e^{-\frac{(n+1)\pi}{2N}j}\sum_{i=0}^{2N-1}e^{\frac{(n+1)2\pi}{2N}ij}] \quad (9)$$

In the formula, from 0 to the sum and from 1 to the sum is the same.

This paper focuses on the study and construction of 12 H-bridge cascade multi-level inverter model, so the following will be based on the above superposition of the calculation process specifically listed in the three operating conditions of the inverter, each H bridge In the power field effect of the turn-on time. So as to fit the sine wave, improve the output waveform, to achieve the design function.

a) 12H bridge full state operating conditions, N = 22, the N into the formula 10, get each H bridge turn-off time, see Tab. 1.

TABLE I 12H BRIDGE CASCADE WORKING STATE

	$0 \sim \pi$ cycle		$\pi \sim 2\pi$ cycle	
H bridge Numbering	***Opening angle***	***Off angle***	***Opening angle***	***Off angle***
1	0.039	179.961	180.039	359.961
2	10.342	169.658	190.342	349.658
3	10.360	169.640	190.360	349.640
4	18.130	161.870	198.130	341.870
5	22.336	157.664	202.336	337.664
6	28.210	151.790	208.210	331.790
7	33.573	146.427	213.573	326.427
8	40.138	139.862	220.138	319.862
9	46.601	133.399	226.601	313.399
10	55.852	124.148	235.852	304.148
11	67.577	112.423	247.577	292.423
12	79.279	100.721	259.279	280.279

b) In the case of a H-bridge fault in the device, under N-bridge operating conditions, N = 21, and N is substituted into Equation 10. Obtain the turn-off time for each H-bridge.

TABLE II 11H BRIDGE CASCADE WORKING STATE

	$0 \sim \pi$ cycle		$\pi \sim 2\pi$ cycle	
H bridge Numbering	***Opening angle***	***Off angle***	***Opening angle***	***Off angle***
1	0.038	179.962	180.038	359.962
2	12.233	167.767	192.233	347.767
3	25.325	154.675	205.325	334.675
4	38.574	161.870	218.574	341.870
5	39.712	140.288	219.712	320.288
6	51.387	128.613	231.387	308.613
7	63.139	116.861	243.139	296.861
8	73.237	106.763	253.237	286.763
9	81.248	98.752	261.248	278.752
10	86.807	93.193	266.807	273.193
11	89.641	90.359	269.641	270.359

c) In the case of two H-bridge faults in the equipment, 10 N-bridge operating conditions, N = 20, N will be substituted into the formula 10. Get each H bridge turn-off time, Table 3.

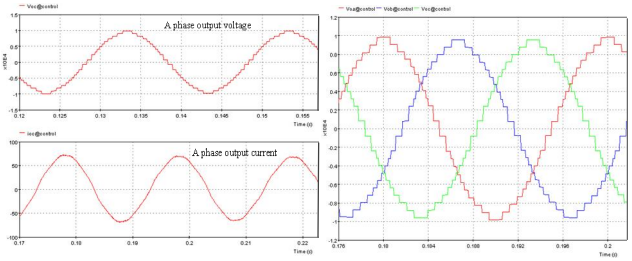
TABLE III 10H BRIDGE CASCADE WORKING STATE

	$0 \sim \pi$ cycle		$\pi \sim 2\pi$ cycle	
H bridge Numbering	***Opening angle***	***Off angle***	***Opening angle***	***Off angle***
1	3.790	176.210	183.790	356.210
2	9.701	170.299	189.701	350.299
3	24.168	155.832	204.168	335.832
4	37.221	142.779	217.221	322.779
5	38.783	141.217	218.783	321.217
6	52.705	127.295	232.705	307.295
7	65.199	114.801	245.199	294.801
8	75.620	104.380	255.620	284.380
9	83.483	96.517	263.483	276.517
10	86.701	93.299	266.701	273.299

IV. SIMULATION AND EXPERIMENTAL VERIFICATION

A. Simulation Research

Application of EMTP simulation software. The 12H bridge cascade model is taken as an example to simulate the H bridge cascade multilevel inverter. Figure 4(a) for the a-phase output voltage, the output current waveform, seen from the figure, the output waveform for the trapezoidal wave to fit the sine wave output, in line with the control strategy.



(a) A phase output voltage and voltage simulation waveform (b) a, b, c three-phase output current simulation waveform

FIGURE IV. SIMULATION FIGURE

Figure 4(b) is a, b, c three-phase output voltage simulation waveform, as shown in the figure, three-phase output voltage are consistent with the principle of multiple superposition method, by the ladder wave superposition, fitting sine wave output, Strategy control to achieve stable output.

B. *Experimental Verification*

In order to further verify the correctness and feasibility of the control strategy, a 12H bridge cascade multilevel inverter experimental device was built and tested on the experimental device. The experimental parameters were consistent with the simulation parameters. Experimental device master chip using STM32F103C8T6, switch tube selection using HM3207B. Figure 5 is a physical photograph of this experimental setup and Voltage waveform which for the abscissa for the time, each cell 5ms.

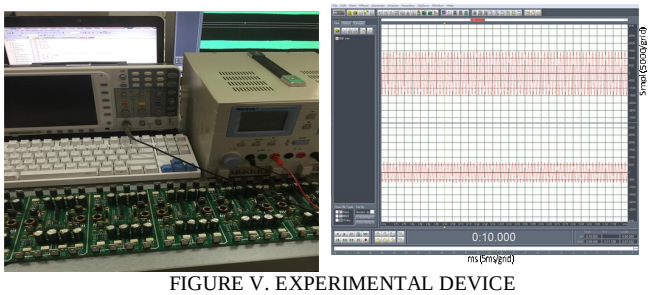
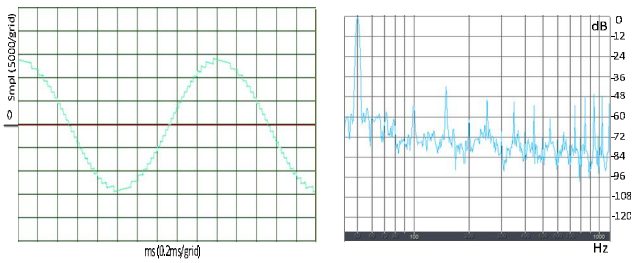


FIGURE V. EXPERIMENTAL DEVICE

TABLE IV EXPERIMENTAL DEVICE PARAMETERS

parameter	Value
Input AC voltage U_s / V	24
Number of cascaded H bridges	12
Switching frequency f_s / kHz	10
Electrolytic capacitor $C / \mu F$	220
Trigger voltage U_c / V	15
Control voltage U_k / V	3.3

Figure 6(a) for the device output voltage waveform amplification, the figure can clearly see the cascade H bridge superposition of the formation of a sine wave, the output of a stable voltage waveform, thus confirming the control strategy described in the article. Figure 6(b) for the output voltage harmonic pattern, the total voltage distortion rate, harmonic content is very small, excellent output waveform, indicating that the topology and control strategy to achieve the inverter function.



(a) A period of voltage wavefor (b) Results of FFT analysis

FIGURE VI. EXPERIMENTAL DIAGRAM

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