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The voltage equalization control method of MMC sub-modules based on packet sorting

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Abstract： When the converter works, the process of charging and discharging frequently can not be accurately controlled，this will cause the voltage imbalance between the capacitor of each sub-module, which leads to abnormal operation of the converter. only to maintain the balance of the sub-module capacitor voltage stability，the converter will operate normally. In the traditional MMC sub-modules voltage equalization method, the switching state of sub-modules is determined by the direction of the bridge arm current and the capacitance voltage size, this will lead to the original sub-modules have to switch again, the frequent changes of the switching status will make a higher switching frequency of IGBT，consequently, the switching losses of the converter are increased. A method of capacitance voltage equalization for MMC sub-modules with optimized switching frequency is proposed，first, the sub-modules of the bridge arms are grouped,and then sorted according to the size of each group voltage, then set the maximum permissible voltage difference between groups， finally, the retention factors are introduced in each group.The optimization method can reduce the switching frequency more effectively while the sub-modules are equalized, thus reducing the switching loss.

1. Introduction

The modular multi-level converter (MMC) is a multi-level converter topology proposed in 2001, the converter valve is composed of many sub- modules in series, as the number of levels increases, the output waveform is closer to the sine wave. High-voltage DC transmission based on modular multi-level converter is the latest achievement of the development of voltage source converter type HVDC technology to high voltage and high power[1].

As can be seen from the MMC topology, each sub-module has a capacitor. When the converter is working, it is impossible to control the charging and discharging process accurately, which will cause the voltage imbalance between the sub-module capacitors, resulting in abnormal operation of the converters. Only to maintain the balance of the sub-modules capacitance voltage stability, the converter can work properly. In fact, the goal of balancing control is not to achieve full consistency of the capacitance voltage of each sub-module, on the contrary, it is necessary to suppress the volatility of each sub-module capacitance voltage relative to its rated value[2].

The voltage equalization control of the sub-modules is related to the modulation mode adopted by the MMC. However, based on the nearest level approximation modulation (NLM) method, the output level of the bridge arm approaches the reference level by selecting the number of sub modules input, it is suitable for occasions where the number of levels is large[3], In document [4], a voltage upper limit and lower limit are set near the capacitor voltage rating, the emphasis of the balance control is the sub-module of the capacitor voltage limit, and then it is sorted according to the over limit condition. In document [5] , the holding factor is introduced so that the sub-modules can keep the original switching state as much as possible to reduce the switching frequency of the device. Hovever, in the above method, the switching frequency of the sub-modules is higher.

This paper presents a method of capacitance voltage equalization for MMC Sub - modules with Optimized switching frequency. The bridge arm modules are grouped so that the number of sub-

modules participating in equalization is reduced, then set the allowable maximum voltage difference ΔU_{max} between groups, finally, the retention factor are introduced between the groups to make the sub-modules as much as possible to maintain the state before. Combining the three methods, the switching losses can be reduced while the capacitance voltage of the sub-modules is balanced, to achieve a better result.

2. The topology and working principle of mmc

Figure 1 is a topological structure of MMC and its sub module. The MMC is composed of multiple sub-modules in series, each sub-module has six arms. The upper and lower arms of MMC are composed of n identical sub-modules and connected in series with a reactance L, each phase has 2n sub-modules, U_{dc} is the DC side voltage. The sub-module is composed of a DC storage capacitor C and a fully controlled type power electronic device IGBT which is complementary to the upper and lower two states. D1and D2 are anti-parallel diodes，U_{SM} is the output voltage of the sub-modules when the MMC is in steady operation. U_C is the capacitance voltage for sub-modules, the effect of the bridge arm reactance L is to suppress the internal circulation between the bridge arms.

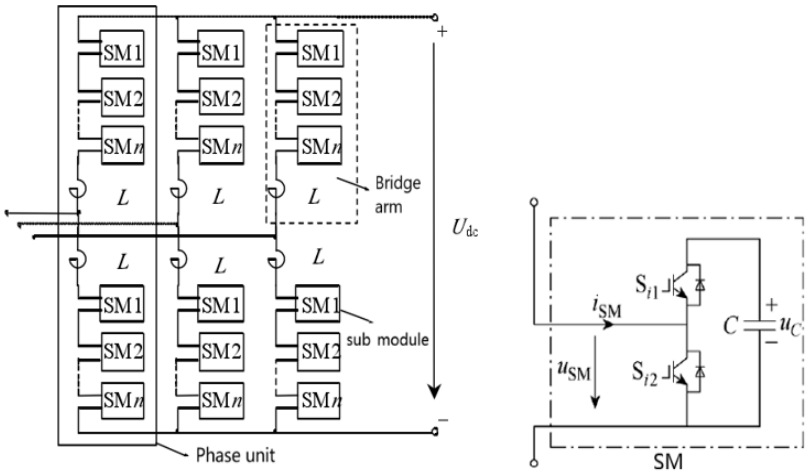

Fig.1. Opological structure of MMC and its sub-module

Because the capacitance of each sub-module is U_C, so each bridge arm can produce a level of 0 to $N.U_C$ size. The basic equivalent circuit of the MMC (in the case of phase A) is shown in figure 2, the upper and lower bridge voltage composed of sub-modules are controlled by a equivalent voltage source U_1 and U_2.

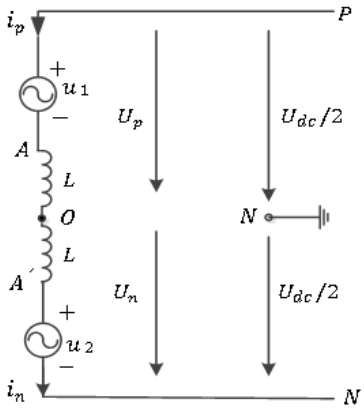

Fig.2. The circuit structure of A-phase

In order to keep the DC voltage stable, it's necessary to meet the conditions:

$$U_p + U_n = U_{dc} \qquad (1)$$

U_p and U_n respectively represent the output voltage of the upper and lower bridge arms, at any moment, the number of sub-modules running in each phase is n. If the number of sub-modules on the upper bridge arm is n_p, the number of sub- modules on the lower bridge arm is n_n, which is satisfied:

$$n_p + n_d = n \tag{2}$$

It can be seen from the figure: there is the following relationship between the A phase output voltage of MMC and the bridge arm voltage:

$$\begin{cases} U_{AN} = -U_1 + \frac{U_{dc}}{2} \\ U_{A'N} = U_2 - \frac{U_{dc}}{2} \end{cases} \tag{3}$$

In addition：

$$\begin{cases} \mathrm{n} \times U_C = U_{dc} \\ U_1 = n_p \times U_C \\ U_2 = n_d \times U_C \end{cases} \tag{4}$$

According to (1) ~ (4) we can see: if the sub-modules of the upper bridge arm are all turned on, then the minimum output voltage of MMC is $-\frac{U_{dc}}{2}$;if the sub-modules of the lower bridge arm are all turned on, then the maximum output voltage of MMC is $\frac{U_{dc}}{2}$.

3. The optimized sub-module voltage equalization method

(1) First of all, each arm of the n (mostly even) sub-modules are divided into k groups on average, so that each group contains two sub-modules, the number of each group is k(k=1，2，3……n/2). When the number of sub-modules that need to be turned on each arm is determined, then the sub-modules that need to be turned on are evenly distributed to each group, it can be described by formula $n_{on} = \frac{n}{2} \times Q + R$. Q represents the base of each sub-module that needs to be turned on , R is based on the size of the capacitor voltage and the current direction of bridge arm, as appropriate, then assigned to the required groups. As we can see, it sorts n sub-modules before grouping, and then sort n/2 groups after grouping, as a result, the sub-modules involved in the equalization are reduced, the amount of computation is also halved, thus, the sorting speed of the capacitance voltage is improved.

(2) After completing the grouping, the voltage U_k of each group is sorted from small to large. In fact, the goal of balancing control is not to achieve full consistency of the capacitance voltage of each sub-module, but to suppress the sub-module capacitance voltage relative to its rating of the volatility. When the grouping is completed, the allowable maximum voltage difference ΔU_{max} between groups is set, when the voltage of each group has a small deviation, there is no need to adjust the results, so as to continue to maintain the current switching state of sub-modules in the group, thereby reducing the device switching frequency. When $U_K \leq \Delta U_{max}$, the switching status of the sub-modules in each group is unchanged, on the contrary, the traditional sub-module voltage equalization method is adopted; when $i_{brg} > 0$, the remainder R is given to the smaller group of U_k, when $i_{brg} < 0$, the remainder R is given to the Larger group of U_k. Finally, the number of sub-modules allocated in each group is less than one, thus, the voltage imbalance between the groups can be avoided.

(3) The retention factor is introduced into the sub-modules in each group to make the sub-modules as much as possible to maintain the state before, when the bridge arm current is positive, then the U_C of the charged modules in the group are multiplied by a holding factor X (X<1), when the bridge arm current is negative, then the U_C of the discharged modules in the group are multiplied by a holding factor Y (Y>1).Then, in accordance with the traditional sorting method to select the input sub-modules, the input sub-modules can be kept as original as possible in the next trigger control so as to effectively reduce the switching frequency. The combination of the three methods can reduce the deficiencies of either method alone, the switching loss can be reduced while the capacitor voltage of the submodule is balanced, to achieve better results.

4 . Simulation verification

In order to verify the effectiveness of this optimized method, a three-phase seven-level MMC model is built in Matlab/Simulink. The parameters used in the simulation are shown in table 1. Since the magnitude of the allowable fluctuation of the capacitance voltage of the sub module is 5% of the rated value, that is 0.15KV. The maximum voltage deviation ΔU_{max} between groups is the sum of the amplitude of the two sub-modules in the group, that is 0.3KV. Taking a sub-module of the upper arm of the A-phase as an example, the trigger signal diagram as shown in figure 3 and figure 4 can be obtained.

Table 1. The simulation parameters in MMC

DC side voltage：U_{dc}	18KV
Number of sub-modules of bridge arm：n	6
Capacitor voltage of sub-modules：U_C	3KV
Sub-module capacitance：C	5600μF
Load Resistance：R	20Ω
Inductance of bridge arm：L	14HZ
Retention factor ：Y	1.01
System frequency：f	50HZ
Retention factor ：X	0.99

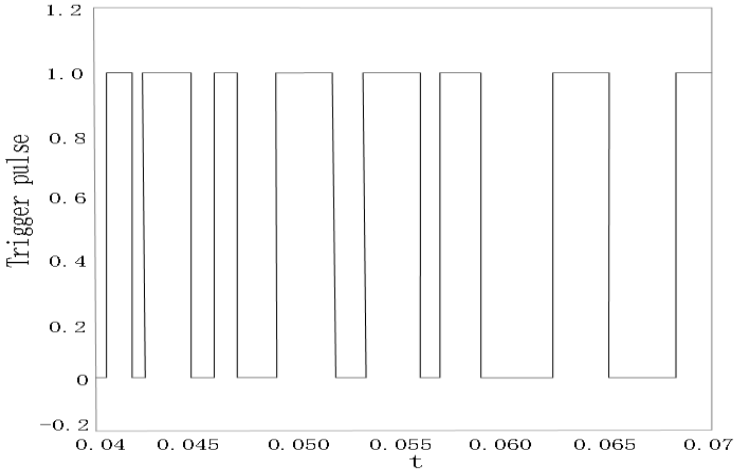

Fig.3. Trigger pulse of sub-modules in traditional voltage equalization method

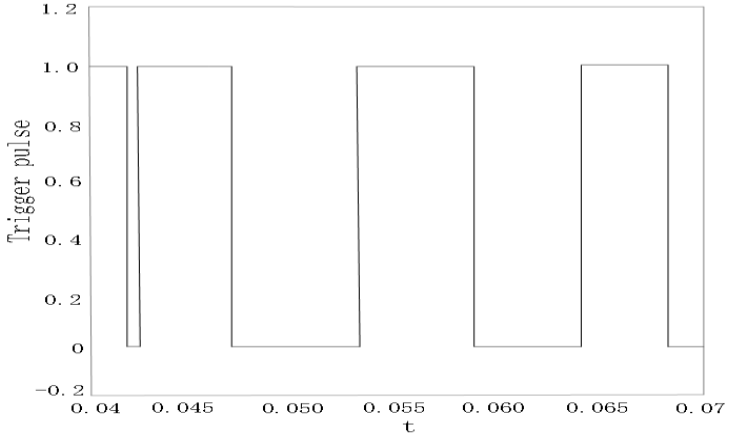

Fig.4. Trigger pulse of sub-modules in optimized voltage equalization method proposed in this paper

Figure 3 is the trigger pulse of sub-modules in traditional voltage equalization method; figure4 is the trigger pulse of sub-modules in optimized voltage equalization method proposed in this paper. From the simulation results we can see that, the switching frequency under the optimized equalization method is significantly reduced, the effectiveness of this method proposed in this paper is proved. Taking the upper bridge arm sub-modules of the A-phase as an example,the capacitance voltage waveform of sub-modules as shown in figure 5 and figure 6 can be obtained

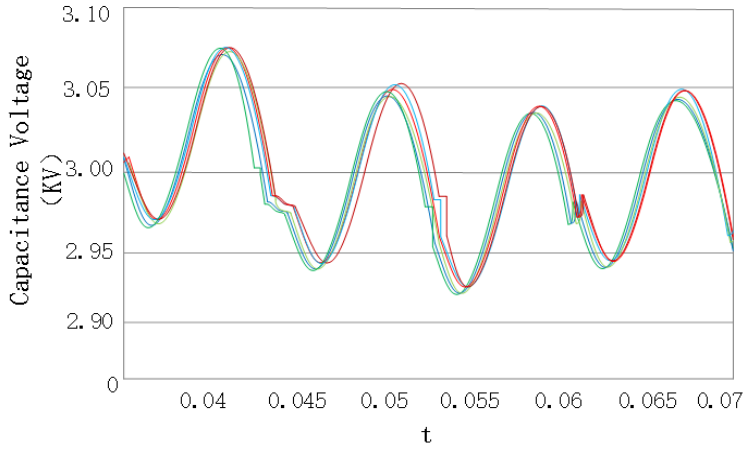

Fig.5. Capacitance voltage waveform of sub-modules in traditional voltage equalization method

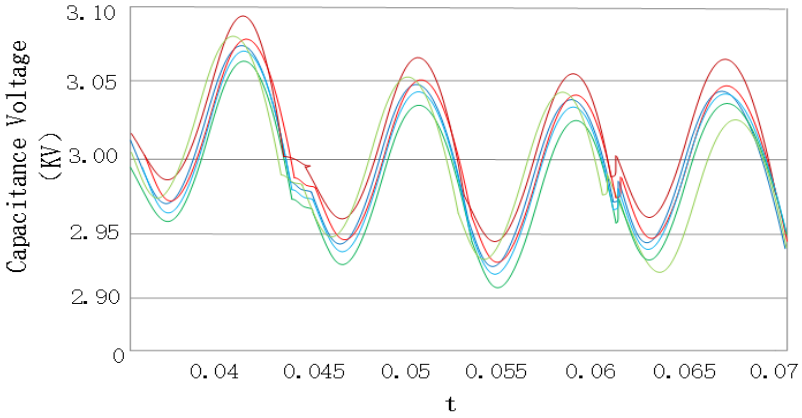

Fig.6. Capacitance voltage waveform of sub-modules in optimized voltage equalization method

Figure 5 is the waveform of the capacitance voltage in traditional voltage balancing method; figure 6 is the capacitance voltage waveform of sub-modules in optimized voltage equalization method .As can be seen from figure 5 and figure 6, the capacitance voltage uniformity of the sub-module under the optimization control method is lower than that of the traditional method, but at the same time, the fluctuation range of capacitance voltage of each sub module is $\pm 3\%$, Within ± 5% of the permissible range of fluctuation, that is, there is no significant impact on the output.

5. Summary

This paper presents a method of capacitance voltage equalization for MMC sub-modules with optimized switching frequency, combining with three methods contained bridge arm sub-module grouping, the maximum voltage difference ΔU_{max} between groups and the introduction of the retention factor. Finally, a model was built in Matlab/Simulink, it is found that the switching frequency is obviously reduced, so the loss will be reduced. Although the optimized sub-module capacitance voltage uniformity is reduced, however, it's effect is very small and satisfies the deviation range, therefore, this optimization method is effective in reducing the switching frequency while realizing the voltage equalization of sub-modules.

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