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Surface Passivation Process Study with Polyimide for High Voltage IGBT

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Abstract. In this paper, high voltage，high power insulated gate bipolar transistors (IGBT) were fabricated with the passivation layer by photosensitive polyimide (PSPI) process. The PSPI was spin coated on a silicon substrate. The soft bake conditions were firstly discussed. In consideration of thermal properties, a temperature hard bake process was carefully optimized. Finally, the polyimide passivation layer was hardened by exposure to nitrogen at 120˚C for 60min+160˚C for 60min+240˚C for 80min+280˚C for 30min+350˚C for 60min. Using this optimized cured process, the outgassing effect in post-fabrication heat treatment can be easily eliminated. Threshold Voltage swings observed on IGBTs power devices before and after H3TRB have been correlated to the presence of a PSPI passivation layer. As a result, it verifies passivation quality of the PSPI layer.

I. INTRODUCTION

Recently, the polyimide (PI), especially the photosensitive polyimide [1], has become increasingly important in semiconductor industry, because of its CMOS capability, outstanding mechanical strength and electrical properties[2], In addition ,the polyimide line resolution is becoming more and more precise, It can be used as an insulator in microelectronics(Fig. 1)[3], dielectrics in flip chip integrated circuit packages [4, 5], substrates in flexible electronic devices [6], neural electrode architecture[7], etc.

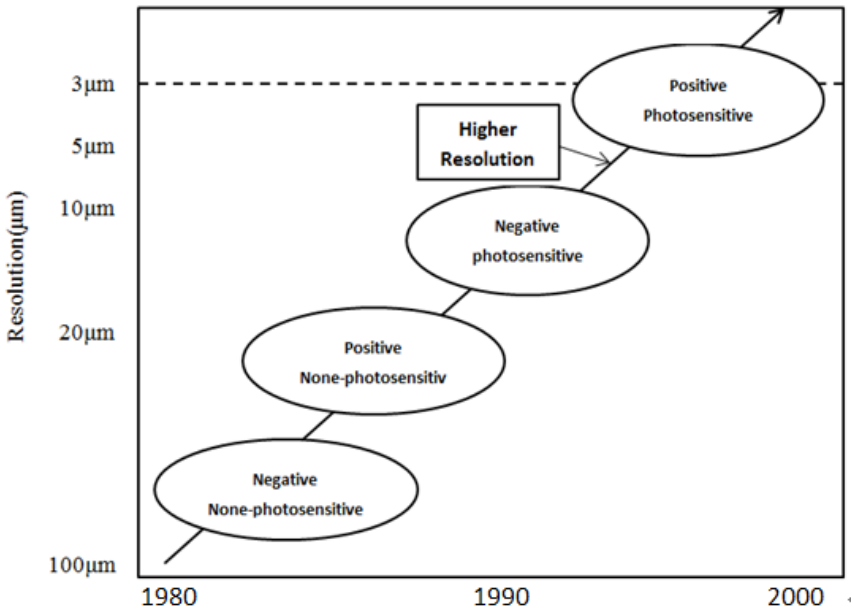


FIGURE 1. Polyimide development trend

As IGBT has developed for several decades, the designs and fabrications of IGBT have become more and more complex, The surface of a semiconductor is very sensitive to high electric fields at the IGBT fabrication process. It is necessary to treat the surface in some way to obtain a well-defined surface and to terminate the free bonds of the silicon atoms at the surface [8].

In this paper, the PSPI is used as the surface passivation of the Si high voltage and large power IGBT. We first optimized the soft bake temperature and the duration. On the basis of the results, the study of surface morphology showed that the PSPI presents an excellent surface conditions in the lithography processing of the power device semiconductor fabrication. In order to reduce the influence of weight loss in thermal treatment, the hard bake parameters were discussed. After hardened by exposure to nitrogen at 120˚C for 60min+160˚C for 60min+240˚C for 80min+280˚C for 30min+350˚C for 60min., the passivation performance of the device is evaluated by H3TRB. The results showed good thermal, chemical and electrical properties which could attract great attention as passivation materials in High voltage and high power IGBT manufacturing technology.

II. EXPERIMENT

Silicon wafers (diameter 6 inches, thickness 500μm, n-type, (100), resistivity 200–400Ω.cm, total thickness variation (TTV) <6μm) were used in these experiments. The process of surface MOS fabrication has been completed by oxidation, photolithography, etching, implantation and metallization (Fig. 2).

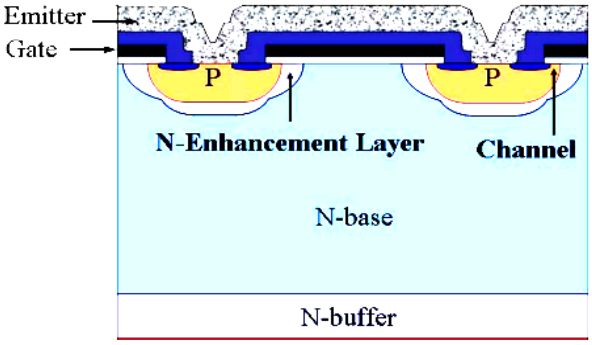


FIGURE 2. IGBT simplified structure

4-5um aluminum is formed on the surface of the device. Photosensitive polyimide was then deposited by spin coating. Photolithography was performed by use of a commercial aligner. The polyimide insulating layer was hardened in an atmospheric ambient at 80˚C for 120min+150˚C for 60min+180˚C for 60min+250˚C for 60min+350˚C for 60min. The PI layer thickness is greater than 20 microns (Fig. 3).

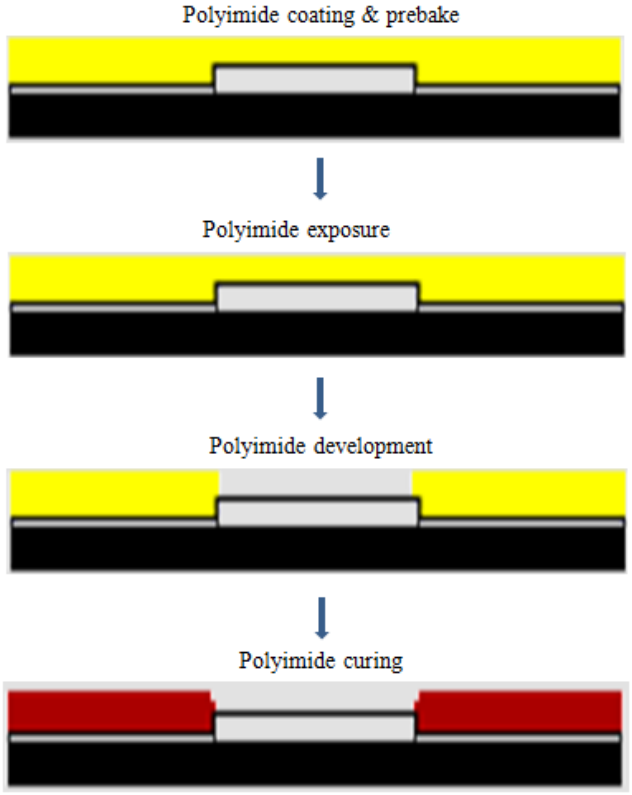


FIGURE 3. PSPI Process simplification

III. RESULTS AND DISCUSSION

Patterning process of PSPI

The purpose of passivation application was the formation of PSPI layer which covered on the metal of the device terminal (Fig. 4). It will prevent the moisture and other pollutants from outside entering the semiconductor surface. As in junction terminations such as the planar structure with potential rings, electrical field peaks occur at the surface, the passivation becomes more crucial. The resulting blocking capability of the device is very sensitive to charges in the passivation layer.

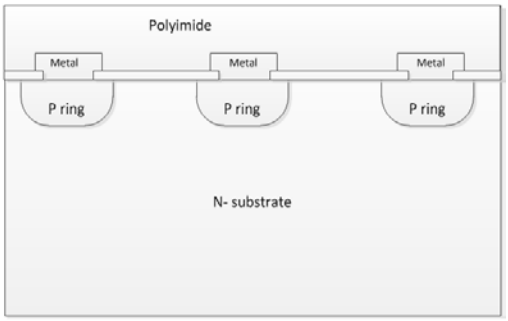


FIGURE 4. Schematic view of the new termination design

However, the formation of PSPI layer usually needs a suitable process to define pattern areas, which often leads to steep sidewalls[9], in order to ensure that the sidewall is covered the layer of metal, were achieved as in Figure 3. The PSPI is firstly spread on the wafer at 500rpm for 10sec and then spin coated at 2000rpm for 30sec. The 500rpm for 10sec to make the PSPI more uniformly distributed over the silicon wafer, and the 2000rpm for 30sec in order to achieve the target thickness. The soft bake parameters were very important for the following lithography process. An insufficient soft bake will result in a very narrow process window for subsequent development . However, if the baking time is too long, the over baked polyimide layer will become very difficult to etch by the developer. If the baking time is too short, the polyimide layer will become easy peeling in the subsequent flows. After the optimization, we found that baking on a hotplate at 80˚C for 6min+ 120˚C for 6min was very suitable for the following lithography process. Table 1 shows the process parameters for patterning PSPI as the passivation layer.

TABLE 1. Three Scheme comparing.

	Patterning Process
Coating	500rpm for 10sec and 2000rpm for 30sec
Soft bake	80℃ for 6min+120℃ for 6min
Exposure Dose	300mJ/cm^2
Exposure tool	g-line
Development	2.38% TAMH, 100s
Hard bake	80˚C for 120min+150˚C for 60min+180˚C for 60min +250˚C for 60min+350˚C for 60min

Hard Bake of PSPI

The hard bake, which was considered as an important process for PSPI formation, was usually performed after development. The purpose of hard bake was to increase the chemical and physical stability of patterned PSPI structures for potential corrosions in subsequent processes, such as electroplating, dry and wet etch. More importantly, the harden process acted as a key process to form the sloped sidewalls.

It can be noted that the sidewalls present a suitable inclination after hard bake. However, the thickness of PSPI decreases from 40μm to 20μm. Since many thermal processes, such as packaging and annealing, will be applied during device fabrication, hard bake was also considered as a necessary process to increase the PSPI thermal resistance.

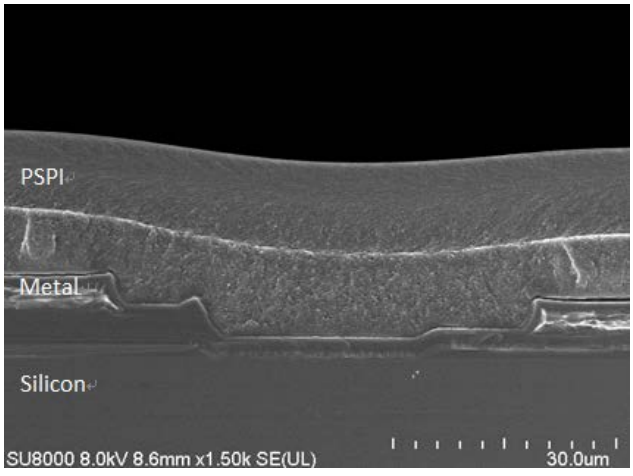


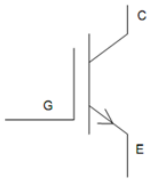
FIGURE 5. SEM scan image of cross-sectional view of polyimide

Since the temperature of heat treatment is higher than that of hard bake, in order to eliminate the outgassing effect, the most straightforward way was to increase the harden temperature. However, the fabrication for microelectronic devices should be achieved at adequately low temperature (typically 350˚C or below) owing to thermal budget limitation, the stress control, or even some alignment requirements. Therefore, we have carefully optimized the harden process at relative low temperature. The polyimide passivation layer was finally hardened in an nitrogen ambient at 80˚C for 120min+150˚C for 60min+180˚C for 60min+250˚C for 60min+350˚C for 60min. Fig.5 presented a SEM image of PSPI surface and metal line surface after the this ladder-like hard bake process.

Reliability test

Threshold voltage (Vth) swings have been observed before and after H3TRB(High humidity/High temperature reverse bias test) (see Table.2).

TABLE 2. H3TRB test flow and conditions

●Pre conditioning MLS3
●Test + Date log 25/85℃

●H3TRB (RH=85% / T=85℃ / bias time = 500/1000 hours /V_{CE}=0.8×V_{CEmax} /V_{GE}=0V)

The applied electrical field during the test acts as a driving force to accumulate ions or polar molecules at the semiconductor surface. On the other hand, the power losses generated by the leakage current must not heat up the chip and its environment and thus reduce the relative humidity. The preconditioning step which reproduces the stresses during the soldering phase of the package on the electronic board, an accelerated reliability test during 500H and 1000H, under severe conditions of humidity ,temperature and electrical bias. Vth is measured at 25℃ after the preconditioning step with a maximum delay of 48h and also after H3TRB test, Fig. 6 shows the result of a H3TRB test with a IGBT module, Vth swings less than 0.1V, the humidity access has been suppressed by the PI passivation layer, according to the failure criteria for acceptance after endurance test (IEC 60747-9) the devices all passed test.

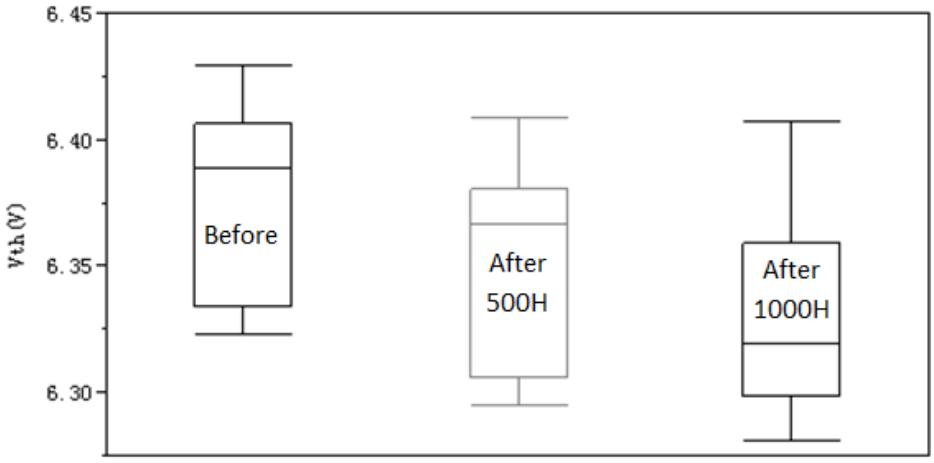


FIGURE 6. Threshold voltage swings before/after H3TRB

SUMMARY AND CONCLUSION

It has been investigated the PSPI based passivation layer application. It can be concluded that PSPI can be used as an passivation layer in high voltage and Large Power IGBT fabrications. By a carefully optimization of harden

process, the outgassing of PSPI in post heat treatment can be eliminated. The SEM scan image showed a suitable PSPI layer for interconnection with other layer. The experimental results also revealed that the IGBT with PSPI layer has passed the reliability test. The PSPI passivation layer presented potential applications to improve power device robustness.

ACKNOWLEDGMENTS

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REFERENCES

1. T. L. Alford, Y. L. Zou, K. S. Gadre, C. King, W. Chen, and D. N. Theodore, "Integration and Electrical Characterization of Photosensitive Polyimide," J. Vac. Sci. Technol. B, vol. 19, pp. 774-779, May-Jun 2001.
2. X. Z. Jin and H. Ishii, "Novel positive-type photosensitive polyimide with low dielectric constant," J. Appl. Polym. Sci., vol. 98, pp. 15-21, 2005.
3. A. Mochizuki and M. Ueda, "Recent development in photosensitive polyimide (PSPI)," J. Photopolym. Sci. Tec., vol. 14, pp. 677-87, 2001.
4. M. E. Grady, P. H. Geubelle, and N. R. Sottos, "Interfacial adhesion of photodefinable polyimide films on passivated silicon," Thin Solid Films, vol. 552, pp. 116-23, 2014.
5. N. Yodo, "Recent development of advanced functional polymers for semiconductor encapsulants of integrated circuit chips and high-temperature photoresist for electronic applications," Polym. Adv. Technol., vol. 8, pp. 215-226, 1997.
6. S. G. J. Coulm, D. Leonard, and F. Bessueille, "Silver localization on Polyimide Using Microcontact Printing and Electroless Metallization," Appl. Surf. Sci., vol. 307, pp. 716-723, Jul 2014.
7. Y. X. Kato, S. Furukawa, K. Samejima, N. Hironaka, and M. Kashino, "Photosensitive-polyimide based method for fabricating various neural electrode architectures," Front. Neuroeng., vol. 5, pp. 11-11, 2012.
8. J.Lutz, H. Schlangenotto, U. Scheuermann et al. "Semiconductor Power Devices: physics, characteristic,Reliablity[M]." New York:Springer Science&Business Media,2011:383.
9. W. W. Flack, G. E. Flores, L. Christensen, and G. Newman, "An investigation of the properties of photosensitive polyimide films," in Optical Microlithography IX, March 13, 1996 - March 15, 1996, Santa Clara, CA, United states, 1996, pp. 169-185.