

Study on Experimental Teaching of Principle and Application of Microcontroller Based on C8051F34X Family

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Abstract—C8051F34X Series MCU using Silicon Labs' patented CIP-51 microcontroller core, fully compatible with the MCS-51 instruction set, and the standard 803x/805x assembler and compiler software could be employed in development. In this paper, the experimental teaching methods and steps of the single-chip microcomputer were introduced based on the characteristics of C8051F34X series MCU.

Keywords—C8051F34X; single chip microcomputer; experimental teaching.

I. INTRODUCTION

The C8051F MCUs utilize Silicon Labs' proprietary CIP-51 microcontroller core with the smallest micro controller package (as small as 2mm x 2mm). The C8051F MCUs are fully integrated mixed-signal System on a Chip MCUs with an internal programmable oscillator ($\pm 2\%$), a true 10-bit (or 12-bit) multi-channel ADC, a voltage reference and built-in temperature Sensor ($\pm 2^\circ\text{C}$). There are also I2C/ SMBus, UART, and SPI serial interfaces implemented in hardware as well as a Programmable Counter/Timer Array (PCA) with five capture/compare modules [1, 2]. The instruction set is mapped to a basic two-stage pipeline to increase throughput while maintaining an 8-bit program memory width. The emergence of C8051F MCUs makes the industry refreshing, so that the majority of MCU system designers saw a new dawn of the MCS-51 MCU [3, 4].

The CIP-51 kernel has all the peripheral configuration of standard 8052, including five 16-bit counter / timer, two full duplex UART, an enhanced SPI port, as many as 4352 bytes RAM, 128 bytes of special function register (SFR) address space and up to 40 I/O pins. The typical structure of the C8051F34X family is shown in Fig. 1.

Different from the traditional SCM Experimental methods, this paper focused on the characteristics of C8051F34X family, and discussed the configuration and main steps of the C8051F34X MCUs.

II. ON-CHIP RESOURCES OF C8051F34X

C8051FF34X family have 10-bit ADCs, high precision internal oscillator ($\pm 1.5\%$), high precision temperature sensor ($\pm 2^\circ\text{C}$), UART, SMBUS/I2C, SPI, controller of USB2.0 which conforms to the USB specification version 2 with resistance and 1KB cache, supporting 8 endpoints, supporting full speed (12Mbps) and low (two 1.5Mbps) modes [5-7]. The resources on the C8051F34X MCU are shown as below.

The C8051F34X core has all the peripherals included with a standard 8052, including five 16-bit counter/timers, 128 byte Special Function Register (SFR) address space, 256 bytes of internal RAM, two full duplex UARTs and 8 (or 4) byte wide I/O Ports. By contrast, the C8051F34X executes 70% of its instructions in one or two system clock cycles, with no instructions taking more than eight system clock cycles. With the C8051F34X MCU's maximum system clock at 50 MHz, it has a peak throughput of

50 MIPS. The C8051F34X MCU has a total of 111 instructions. The table 1 shows the total number of instructions that for execution time [8-10].

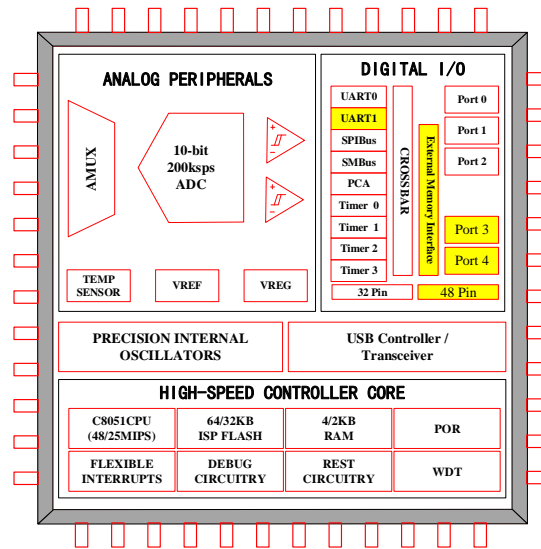


Fig. 1. Typical structure diagram of the C8051F34x family

TABLE I. THE TOTAL NUMBER OF INSTRUCTIONS AND THE REQUIRED EXECUTION TIME

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Numbers of Instructions	26	50	6	16	7	3	1	2	1

III. C8051F34X MEMORY

The memory organization of the C8051F34X System Controller is similar to that of a MCS-51. There are two separate memory spaces: program memory (ROM or FLASH) and data memory (RAM). Program and data memory share the same address space but are accessed via different instruction types, The Memory Map for 64 KB C8051F34x MCUs is shown in Fig. 2.

A. Program Memory

The C8051F34x CPU has a 64 KB or 32KB FLASH memory in system programming. The C8051F34x implements 64k or 32k bytes of this program memory space as in-system, re-programmable Flash memory. Note that on the 64k versions of the C8051F340/2/4/6, addresses above 0xFBFF are reserved.

B. Data Memory

The C8051F34X CPU includes 256 of internal RAM mapped into the data memory space from 0x00 through 0xFF. The lower 128 bytes of data memory are used for general purpose registers (SFR) and temporary storage. Either direct or indirect addressing may be used to access the lower 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode.

The upper 128 bytes of data memory are accessible only by indirect addressing. This region occupies the same address space as the SFR, but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the CPU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory.

C. Special Function Registers (SFR)

The direct addressing memory spaces from 80H to FFH constitute SFRs; The SFRs provide control of the resources and peripherals of the C8051F34X family of single-chip microcomputer. In addition to the 21 SFR in standard 8051, the C8051F34X family adds some SFR to configure and access proprietary subsystems.

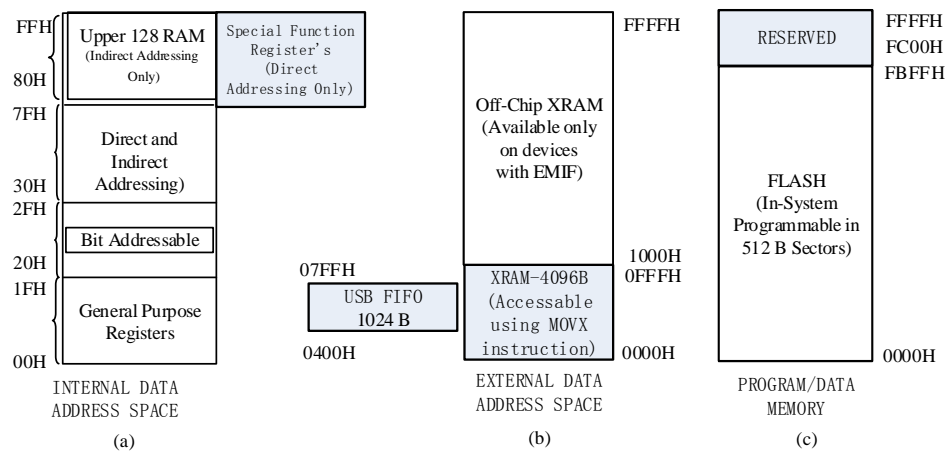


Fig. 2. On-Chip Memory Map for 64 KB C8051F34x MCUs

TABLE II. ABSOLUTE MAXIMUM RATINGS

Parameter	Conditions	Min	Type	Max	Units
Ambient temperature under bias		-55		125	°C
Storage Temperature		-65		150	°C
Voltage on any Port I/O Pin or RST with respect to GND		-0.3		5.8	V
Voltage on VDD with respect to GND		-0.3		4.2	V
Maximum Total current through VDD and GND				500	mA
Maximum output current sunk by RST or any Port pin				100	mA

IV. ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings of C8051F34X family is shown in table 2. Exceeding the parameters in the table may cause permanent damage to the device. Work may affect the reliability of the device over a long period of time at the maximum allowable value or exceeding the maximum allowable value.

V. DEBUG INTERFACE AND EXPERIMENTAL METHODS OF C8051F34X FAMILY

C8051F34x MCUs include an on-chip Silicon Labs 2-Wire (C2) debug interface, allowing Flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system.

The C2 protocol allows the C2 pin to be shared with the user function so that in-system debugging and programmed in FLASH may be performed. It is possible because C2 communications is usually performed in the stop state of the device, where, all on-chip peripherals and user software are stalled. In this halted state, the C2 interface can safely 'borrow' the C2CK (the normal mode is /RST) and C2D (the normal mode is P3.0) pins. In most cases, external resistors are needed to isolate the C2 interface and user applications. A typical isolation configuration is shown in Fig. 3.

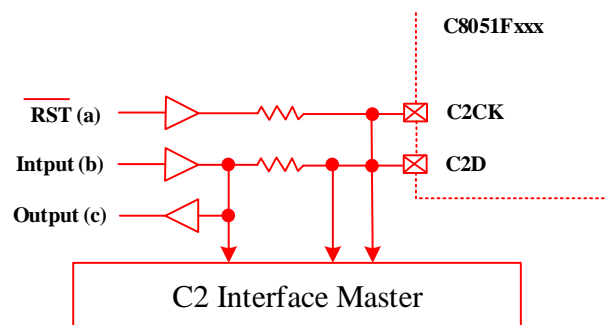


Fig. 3. Typical C2 pin sharing

VI. IDE INTERFACE (INTEGRATED DEVELOPMENT ENVIRONMENT, IDE)

Silicon Laboratories IDE is an integrated development environment developed by Silicon Laboratories Company especially for C8051F microcontroller. It provides all the tools for development and test project for the designer. The whole integrated development environment provides complete project management and development debugging function. It provides a powerful interface for SCM development by using C51 language through integration with C51 series development tools.

C8051F34X MCUs are designed with debugging circuit, the circuit debugging information acquisition chip microcontroller through the boundary scan mode, connected through the C2 interface and development tools of 2-wire, allowing Flash programming and in-system debugging with the production part installed in the end application. Using the IDE debugging environment provided by Silicon Laboratories or the uVision2 debugging environment of Keil, you can perform non-intrusive, full speed system programming (ISP) and debugging.

It is feasible and effective to achieve the purpose of non-intrusive, full speed system programming (ISP) and debugging with the IDE debug interface or the uVision2 debug interface of Keil.

VII. SUMMARY

C8051F34X family utilizes Silicon Labs' patented CIP-51 microcontroller core, which fully compatible with the MCS-51 instruction set, so the standard 803x/805x assemblers and compilers can be used to develop software. C8051F34x MCUs have an on-chip Silicon Labs 2-Wire (C2) debug interface, allowing Flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. Different from the traditional SCM experimental methods, this paper focused on the characteristics of C8051F34X family, and discussed the configuration and main steps of the C8051F34X MCUs. It is proved that the full speed system programming (ISP) and debugging with the IDE debug interface or the uVision2 debug interface of Keil is very convenient and effective.

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