

# A Low Power 28 Gb/s $2^{7-1}$ PRBS Generator and Check with Correlate Dual Outputs in 40 nm Technology

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**Abstract**—A 28 Gb/s PRBS generator and checker with correlation Dual outputs is presented in this paper, with the proposed dual outputs interleaved structure, the PRBS has only the half data rate, which is able to expand the communication data rate. A hybrid counter is proposed to undertake both high frequency and low frequency signal, the proposed PRBS generator and checker has been designed in TSMC 40 nm CMOS 1P9M technology, post-simulation results confirm that can output 28 Gb/s data, the check and counter can work, the power dissipation is 1.5  $\mu$ W.

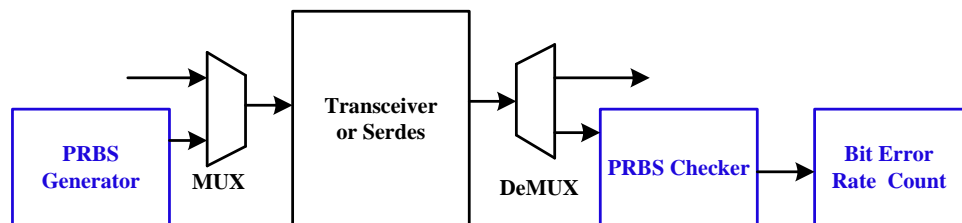
**Keywords**—BIST; PRBS; LFSR; generator; checker; dual-output

## I. INTRODUCTION

Pseudo random bit sequences (PRBS) are fundamental blocks for testing all kinds of digital data communication, it

can measurement the chip bit error rate (BER) with built in self-test (BIST). Most of communication chip products such as transceivers, serdes and fiber optics include PRBS, so the quality of chip can be checked by itself. The check efficiency is increased by eliminate the steps that connect the arbitrary waveform generator (AWG) and oscilloscope [1, 2].

The BIST consists of PRBS generator, PRBS checker and BER counts, Figure.1 shows the architecture of transceiver with built in self-test. PRBS generator produces the pseudo random signal which is sent into the device being tested, on the output side of the transceiver, a PRBS checker recreates the same pseudo random signal as the generator and compares it with the output of the transceiver to find errors.



Transceiver with Built-In Self Test

Figure 1. Transceiver with built in self-test

## II. SYSTEM ARCHITECTURE

PRBS generators are expected generate random sequences as white noise, we can't get noise in digital circuit, but linear feedback shift register (LFSR) circuits can produce the signal which is similar to random noise in some statistic characteristics, but the signal can be repeated, it is called pseudo random bit sequences [2, 3, 4].

Actually, LFSR are finite state machines (FSM), there are  $2^n - 1$  states in an  $n$ -bit LFSR. The state of all the DFF outputs are "0" is removed for avoiding idle. The maximal length of LFSR is  $2^n - 1$  with the primitive polynomial. Table.I shows the typical primitive polynomial. The 7-bit

LFSR architecture is shown in Figure.2, it consists of 7 DFFs and a XOR gate.

TABLE I. TYPICAL PRIMITIVE POLYNOMIAL

Bits	Primitive polynomial.	PRBS Length
7	$x^7 + x^6 + 1$	$2^7 - 1 = 127$
15	$x^{15} + x^{14} + 1$	$2^{15} - 1 = 32767$
31	$x^{31} + x^{28} + 1$	$2^{31} - 1 = 2,147,483,647$

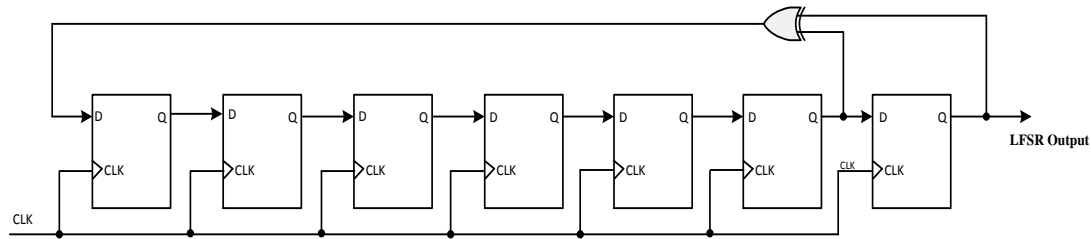


Figure 2. 7-bit LFSR PRBS generator architecture

The PRBS checker is similar to the generator, it eliminates the feedback and does XOR operation between the input signal and the feedback signal. And the check will be

zero if the input signal is still PRBS sequences without being damaged. The 7-bit PRBS checker is depicted in Figure 3.

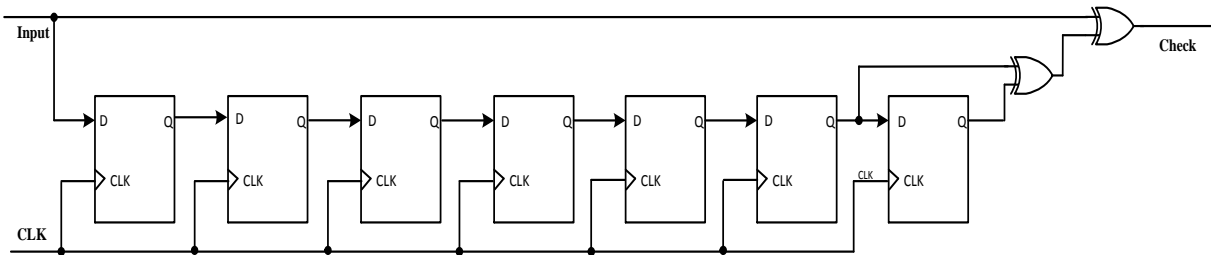


Figure 3. 7-bit LFSR PRBS checker architecture

In order to obtain two correlated output sequences, a two phase interleaved LFSR structure is shown in Figure 4, the DFFs are split into two groups which contain 7 DFFs, the feedback is realized by an XOR gate working as modulus 2 adder, the feedback signal is built from top tap 6th DFF and the bottom tap 7th DFF, and the other feedback is built from bottom tap 6th DFF and the top tap 7th DFF [3, 5].

The top DFFs should be set and the bottom DFFs should be reset initial, so the two correlated outputs will be not alike. The two taps LFSR won't be in all zero state since its interleaved structure. What's more, the LFSR won't be in all zero state as long as one of the DFF is "1". The 7-bit two phase interleaved LFSR is depicted in Figure 4.

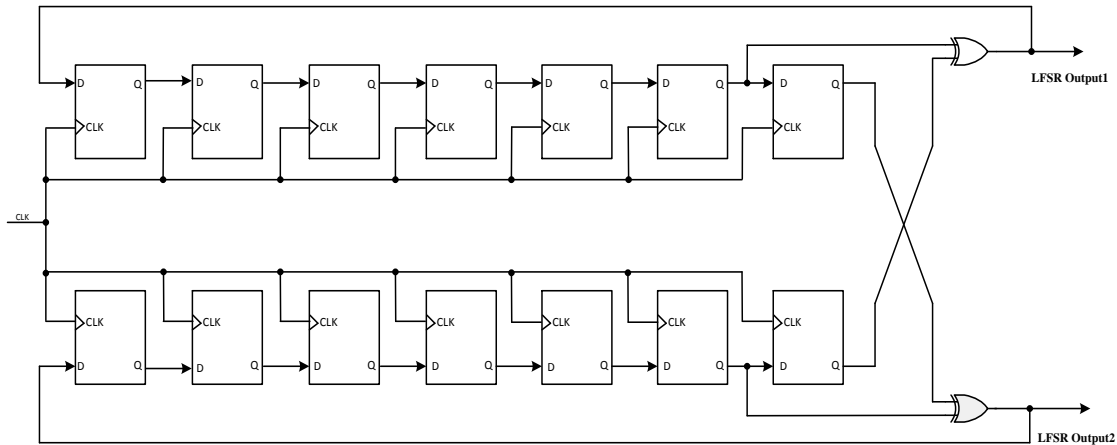


Figure 4. 7-bit two phase interleaved LFSR architecture

### III. IMPLEMENTATION OF CIRCUIT

#### A. PRBS Generator

A 31-bit 2x14Gb/s two phase interleaved PRBS generator is presented, the complete schematic is depicted in Figure 5, the 31-bit two phase interleaved correlate

outputs PRBS generator is built by 31 true single phase clock (TSPC) DFFs which have SET function, 31 TSPC DFFs which have RESET functions and two XOR gate.

What's more, two DFFs are utilized for output, and clock loading is taken into consideration, the SET signal is split into SET and RESET. Four inverters are added for adjusting the cross voltage in eye diagram [5, 6].

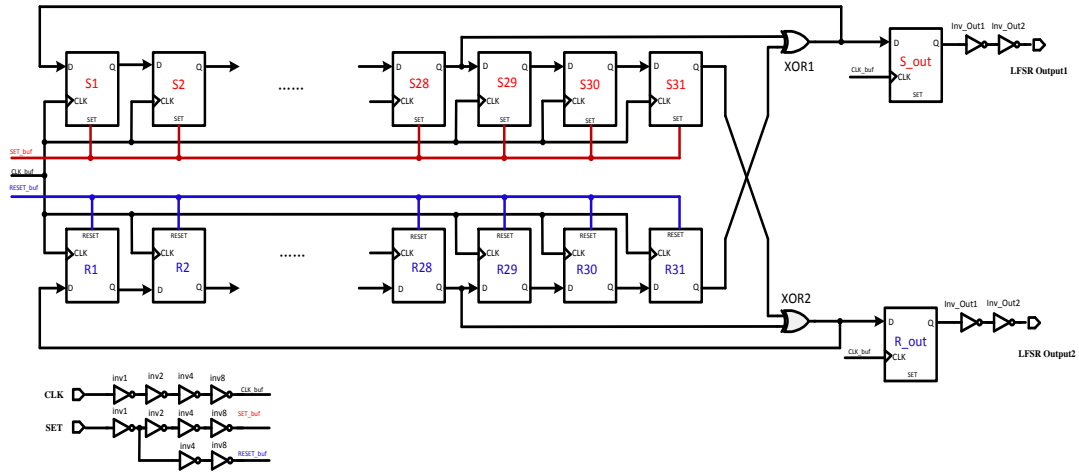


Figure 5. The complete schematic of PRBS generator

### B. PRBS Checker

A 31-bit 2x12.5Gb/s PRBS checker is presented, the theory of PRBS checker is recreate PRBS signal, if the received signal has not been damaged, the sequences is equal to LFSR sequence, so the checker is zero. If we eliminate the feedback and do xor operation between the

input signal and the feedback signal, then the checker is done.

Two DFFs are added to eliminate the effect of delay, what's more, the two checker do or operation then count the error number rather than count the two checker error respectively and then do sum operation, it is uncomplicated compute without losing the function. The complete schematic is depicted in Figure.6.

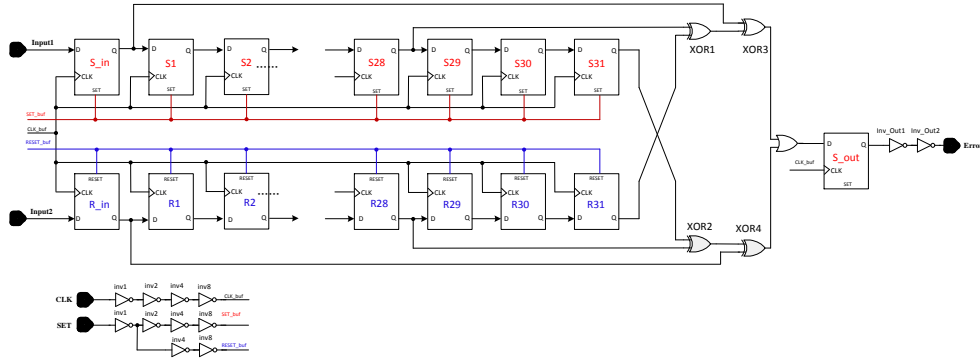


Figure 6. complete schematic of PRBS checker

### C. PRBS BER Counter

The PRBS BER Counts is presented, in order to count 1012 data, the count width must larger than 1012, the counter width n is shown in Eq. 1.

$$n = \log_2 10^{12} \quad (1)$$

Thus count width n is set to 40, the divided by 2 asynchrony count structure is applied. The frequency of DFFs in count vary from 12.5GHz to 12.5 mHz, TSPC DFF is not suit for this count, the ordinary digital TSMC 40nm GP library DFCND1BWP is chosen. CLK\_Enable and Error\_Enable are added to enable the counts, the complete schematic is depicted in Figure.7.

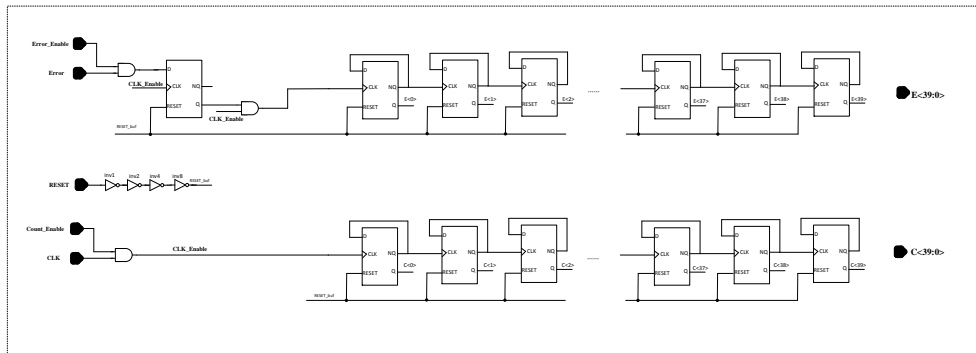


Figure 7. The complete schematic of BER counts

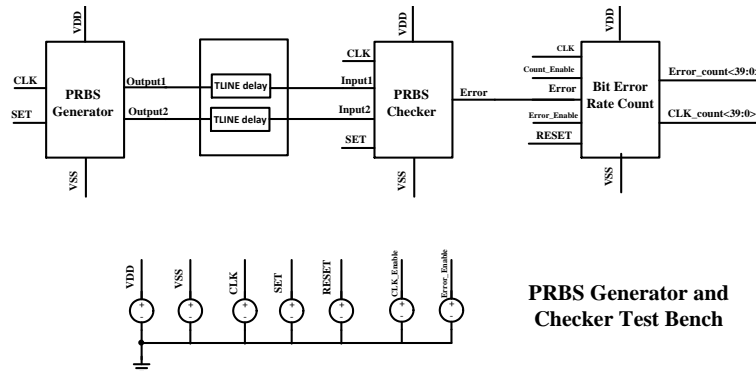


Figure 8. PRBS generator and checker test bench

The whole simulation test bench is established as depicted in Figure.8, the TLINE is utilized to imitate the photonic transceiver, the delay time is set to10ns. The PVT should be take careful because the frequency is too high, and the performance is sensitive to the corners, voltage and temperature.

The proposed 28 Gb/s 27-1 PRBS generator and check has been designed in TSMC 40 nm CMOS 1P9M process. The chip layout is shown in figure.9, and the chip area is 60μmx70μm without test pads.

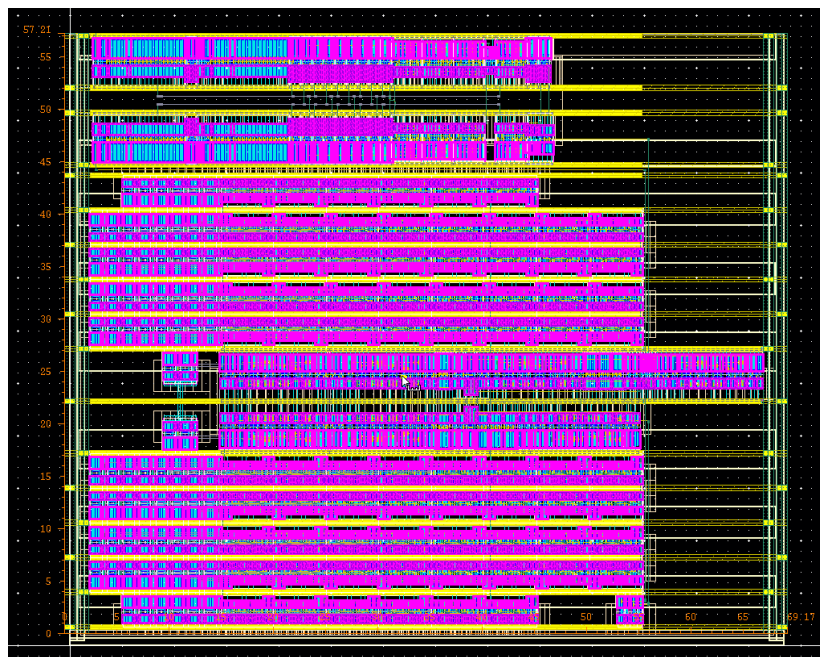


Figure 9. Layout of PRBS generator and checker

The post-simulation results of the two outputs is shown in Figure.10, they are two correlate PRBS output streams, the rise and fall time are 6.5ps and 4.7ps respectively.

The eye diagram of the output stream is depicted in Figure.11 (a), the signal data is from 5.1ns to 100.1ns, the period is 240ps, and the cross voltage is 540mV. The jitters

is 17fs, it exhibits the high performance of PRBS generator. Figure.11 (b) shows the result of checker, the checker is 1 initial for setting all the DFFs, and the checker always be "0" as long as the input of checker is PRBS generator signal.

It shows the BER error count, the count is always "0" for no error happened. And the power is 1.5uW.

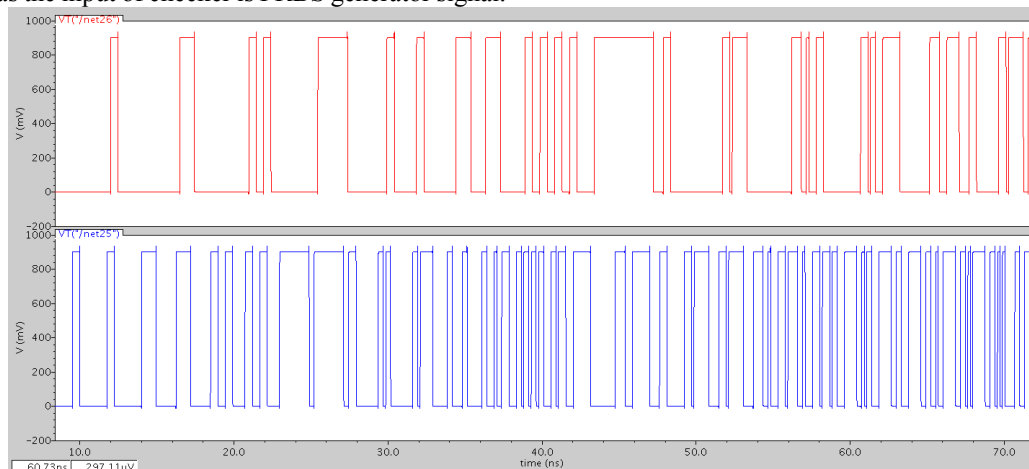


Figure 10. The two correlate output streams

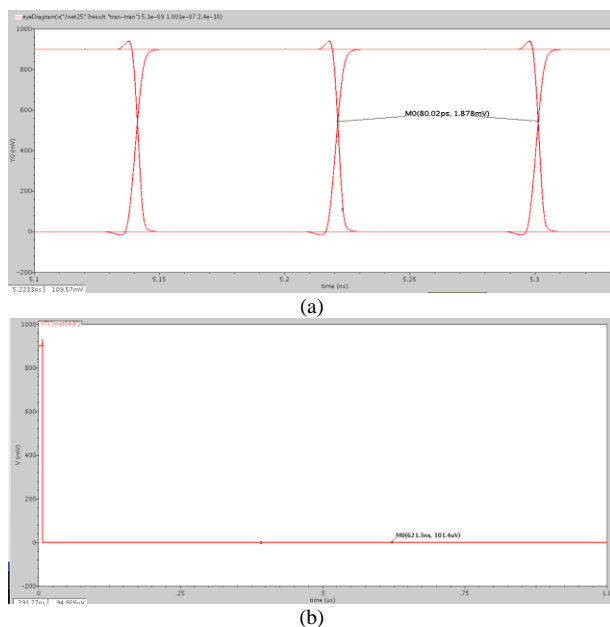


Figure 11. Post-simulation result. (a) eye diagram of PRBS out stream (b) check and counter of PRBS

#### IV. CONCLUSION

A low power 28 Gb/s 27-1 PRBS generator and check with correlate dual outputs is presented in this paper, the novel interleaved LFSR chain is proposed, this method can decrease the half of PRBS data rate, thus CMOS logic circuit achieves a high data rate PRBS in CMOS process

other than Bi-CMOS process. In order to handle high frequency and low frequency clock signal, a hybrid counter is employed.

The proposed PRBS generator and check has been designed in TSMC 40 nm process, the post-simulation results shows that the PRBS can produce 28 Gb/s signal, the check and BER counter can work, and this chip is able to maintain the high performance with 1.5  $\mu$ W power dissipation.

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