

A Multi-channel High Efficiency Boost LED Backlight Driver with High Dimming Ratio

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Abstract—In recent years, the screen size and backlight brightness have been increased year by year in portable electronic equipment, which makes much more requirements for LED driver chips. A 3-channel boost LED driver with high efficiency is proposed, and it has 3 channels with 10 LED lights in each channel. The current flow in each channel can reach to 20mA. In order to improve the output efficiency of the chip, the on-resistance of the power MOS sampling method is used here. Thus can achieve powerless sampling. Direct PWM control method is used in the circuit to complete the dimming, which can achieve colorless output of the white light. The use of a dimming MOSFET and LDO in the circuit to further optimize the power consumption. The circuit is designed and simulated in CSMS 0.25um BCD technology. The input voltage range is 2.7V~5V. The maximum dimming output voltage is 36V. The final output efficiency of the chip

can achieve 91.4%.The rising time of the LED current in the dimming circuit is about 192ns and the falling time is about 14ns. The maximum dimming ratio is 9000: 1 at 500Hz.

Keywords—LED driver; high dimming ratio; high efficiency

I. INTRODUCTION

White light LED is widely used in a variety of portable electronic devices as the first choice of the backlight for small LED screens[1]. And with the screen size of the equipment is larger and larger, how to make the consumption be the lowest is an important thing in designing a driver chip.

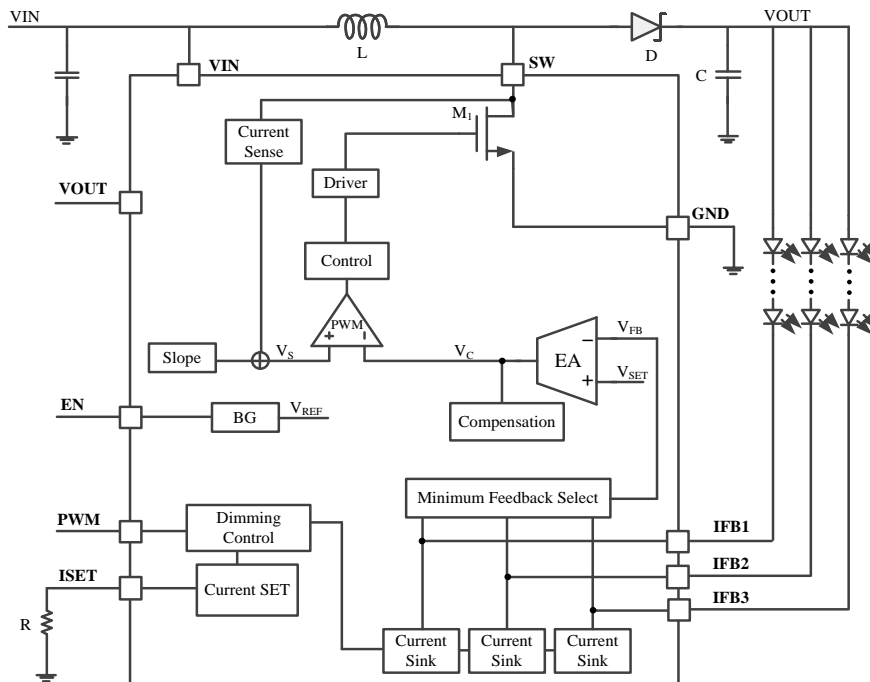


Figure 1. Graph of multiple-channel LED driver system.

A high efficiency boost LED driver chip is proposed in the paper. The turn-on drop voltage is generally 3-4V and conduction current is 20mA. The multi-channel LED driver chip system architecture diagram is shown in Figure 1. The chip internal system lists in the rectangular frame, the external necessary chip devices are listed out of the

rectangular frame. Three channel of LED are tied to VOUT, each current channel of the LED complete the current feedback flow through into the chip IFBx, this circuit can be achieved up to 3 channels, with 10 LEDs in each channel, each channel is regulated by the system respectively to achieve high matching multi-channel LED driver. The

direct PWM dimming is used in the paper, so that the output current can be colourless.

II. CIRCUIT IMPLEMENTATION

A. Current Sense Circuit

The current sampling circuit is an important part in the peak current mode DCDC converter. The inductor current is collected by the circuit and changed into voltage signal, it is needed to compare with the feedback voltage cycle by cycle, thus the power MOSFET duty cycle signal can be

gained. Typical current sampling can be divided into full-cycle sampling and half-cycle sampling. For this design, this paper only need to collect peak current in the inductor because it works in peak current mode control.

There are a lot of methods in current sampling, such as inductance series resistance technique, power transistor on-resistance sampling, senseFET sampling and so on[2]. Considering the output efficiency, the method of power transistor on-resistance is used in the paper, this method has the advantage of no additional loss in sampling, and the disadvantage is the output accuracy is not much high.

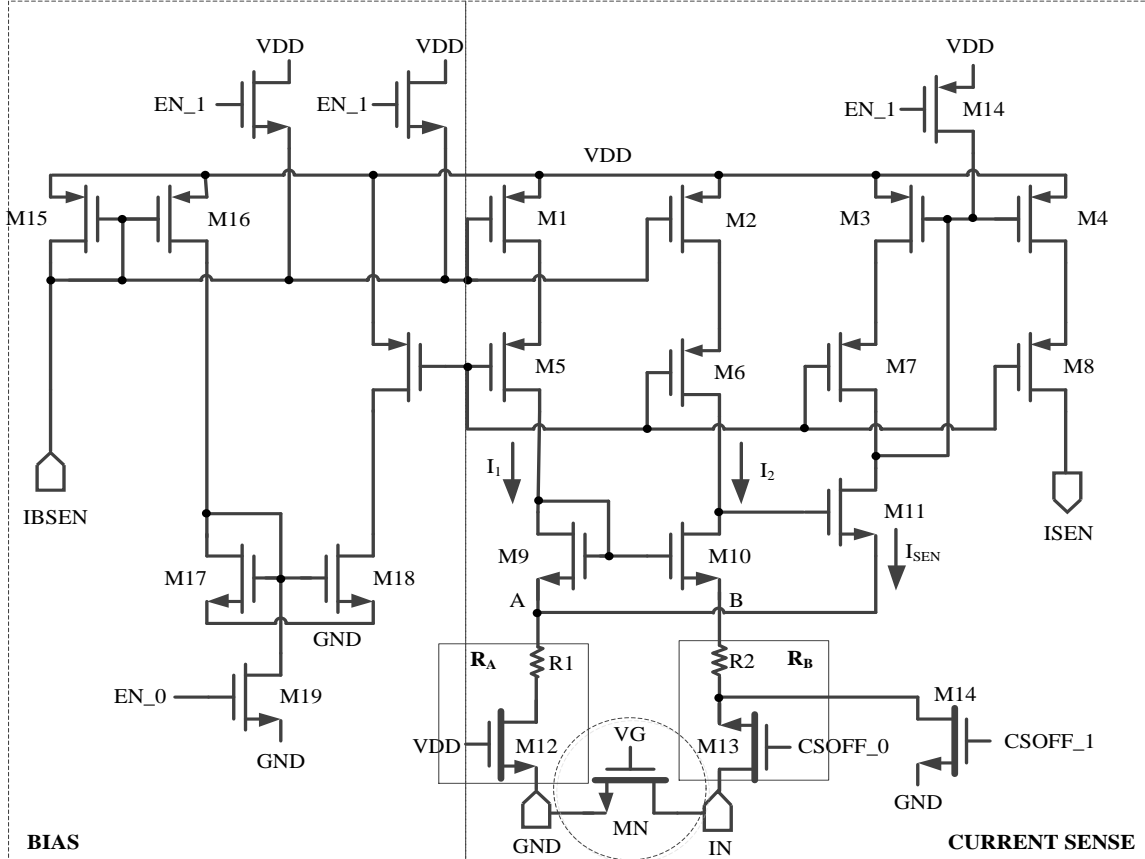


Figure 2. Graph of transistor-level of current sampling circuit.

The transistor-level of current sampling circuit is shown in Figure 2, the left part of the circuit is the bias part, the right part of the current is sampling circuit for the specific implementation. MN, M12, M13, M14 are High-Voltage (HV) MOSFETs in the circuit, because the potential at IN node is very high when power MOSFET MN is turned off. In addition, M12 and M14 are the same size with HV M13 for matching. In the sampling phase, the input pins GND and IN are connected to the source and drain of the power MOSFET MN, respectively. The voltage of CSOFF_0 is high, and the voltage of CSOFF_1 is low, M12, M13 is on, M14 is off. The current mirror composed of M1, M2, M5, M6 to ensure the current I_1 , I_2 flow through MOSFET M9, M10 are equal. In Figure 2, the resistor of R1 and R2, and the MOSFET M12, M13 are all exactly matching in size. Suppose the sum of on-resistor in M12 working in linear region and R1 is R_A , the sum of on-resistor in M13 working in linear region and R2 is R_B . It is got:

$$R_A = R_B \quad (1)$$

And it has:

$$V_A = R_A \times (I_1 + I_{SEN}) \quad (2)$$

$$V_B = R_B \times I_2 + R_{ds} \times I_L \quad (3)$$

Where I_{SEN} is the sampling current, R_{ds} is the on-resistance of the power MOS tube MN, and I_L is the inductor current flowing through the power MOSFET. Since the current of source current I_2 flowing through the power MOS transistor MN is smaller than I_L , and it can be ignored. Simultaneous above, it is drawn:

$$I_{SEN} = \frac{R_{ds}}{R_B} \times I_L \quad (4)$$

The scaling factor for the inductor current of the sampling circuit is gained.

When I_{SEN} flows through resistor R_s and V_{SEN} can be got, it can be gained:

$$V_{SEN} = I_{SEN} \times R_s = \frac{R_{ds}}{R_B} \times I_L \times R_s \quad (5)$$

If $R_s = R_B$, it has:

$$V_{SEN} = R_{ds} \times I_L \quad (6)$$

B. Design of the Low Voltage Drop without Current Overshoot PWM Dimming Circuit

The traditional PWM dimming circuit is shown in Figure 3 [3]. there are a lot of problems in traditional direct PWM dimming: on the one hand, three devices are needed to place under the white LED string: dimming MOS, LDO regulator, and LDO feedback resistor, these devices series will produce power consumption. The total voltage drop of the three devices is about 1V, the dimming MOS and LDO feedback resistors consumption is 0.3V, and the LDO regulator consumption is 0.4V, which costs much power in the entire LED driver chip. On the other hand, the traditional PWM dimming circuit can directly turn off the LED string by dimming MOS, but when the LED string is turned on, the feedback voltage on the resistor is low, and the LDO regulator works in the linear area, and at the moment of MOS on, it will be overshoot in LED current, and it costs a certain time to make the current steady.

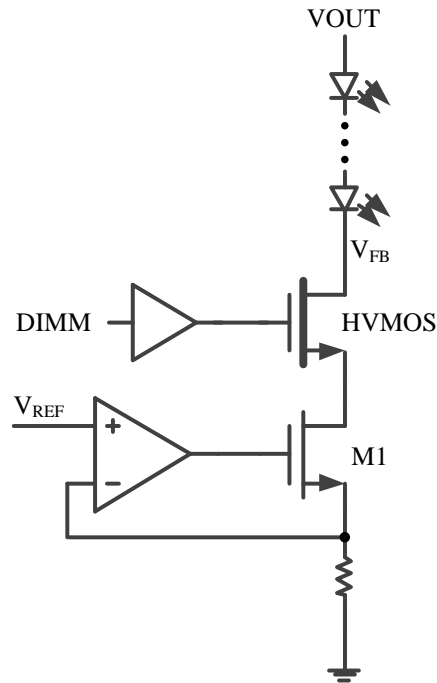


Figure 3. Traditional direct PWM dimming structure

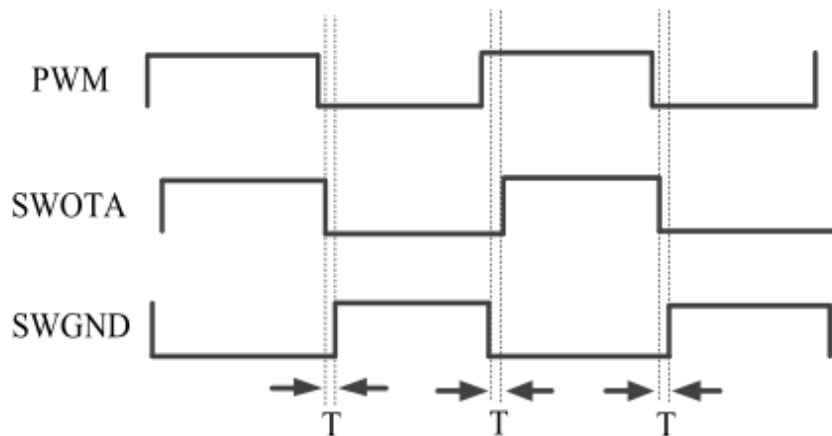


Figure 4. The PWM input control signal waveform.

There is current overshoot problem in traditional direct PWM dimming, on the one hand it is easy to exceed the maximum current limit, which makes LED bad, on the other hand, it is easy to accure brightness instability, and inaccurate in light output in LED. the cause of overshoot is that when the HV MOSFET is down, source voltage in M1 is zero, and the output gate voltage is high potential

compared with VREF. Thus lead M1 works in linear area and totally on. When the dimmer HVMOS is turned on, there is a direct path from VOUT to ground. The instantaneous current increases in LED causes current overshoot. After that, the LDO detects the resistance drop across the resistor and adjusts the loop to complete the current stabilization.

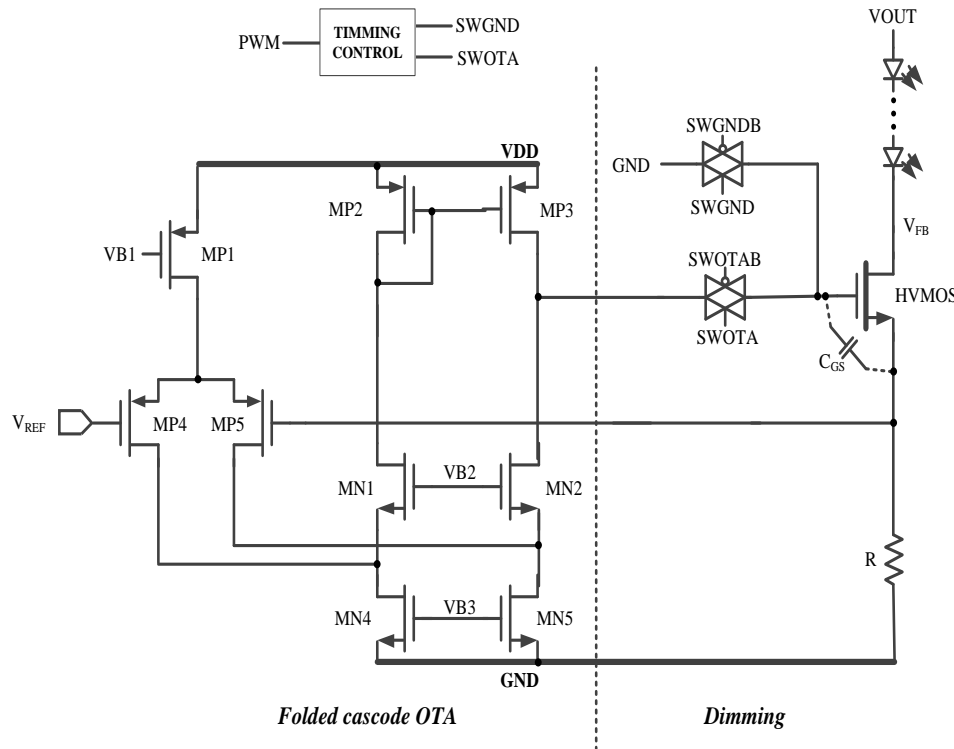


Figure 5. Graph of low voltage no current overshoot PWM dimming circuit.

In order to reduce the power consumption of the dimming circuit and solve the current overshoot problem of the traditional PWM dimming, A PWM dimming circuit without independent dimming MOS is proposed. The PWM input control signal waveform is shown in Figure 4. The transistor-level circuit is shown in Figure 5. The circuit of folded cascode structure OTA is on the left. The positive pole is tied to reference voltage, the negative pole is tied to feedback resistor R, and negative feedback structure is composed. The LDO regulator and dimming MOSFET are both worked by HVMOS. the PWM input waveform is transferred to control to complete HVMOS function in Figure 5.

The work process of the dimming circuit is as follows: a high non-overlapping signal is produced by PWM to control the regulator MOSFET. When the SWOTA signal is in high potential, the output of OTA is connected to HVMOS, thus the LDO feedback control loop is formed and a stable output current is got. But when the SWOTA signal is in low potential, signal SWGND will not transfer to high potential immediate but a little delay in time is formed to prevent a short circuit through the two transform MOSFET. And thus an external computation is got, and

when the SWGND signal goes high, the gate-source capacitance CGS of the HVMOS tube is discharged through the transmission tube to the ground and immediately shut down it. In the same way, when SWGND signal goes low, potential the SWOTA needs to get through a small delay and then on to prevent the leakage. and then, SWOTA once again get into a high potential, CGS is recharged by OTA. And stable current is gained by regulating the HVMOS.

III. MEASUREMENT RESULTS

The current sampling circuit simulation waveform is shown in Figure 6. The waveform above is the inductor current waveform, in the middle is the output current sampling circuit, and the following is the sampling voltage waveform caused by current flowing through RS. RST1 is the sampling circuit reset signal, and the current sampling control circuit only collects the rising phase of the inductor current. The collected Vsen waveform is basically consistent with the inductor current waveform flowing through the power NMOS transistor. This shows that the design of the current sampling circuit is working properly.

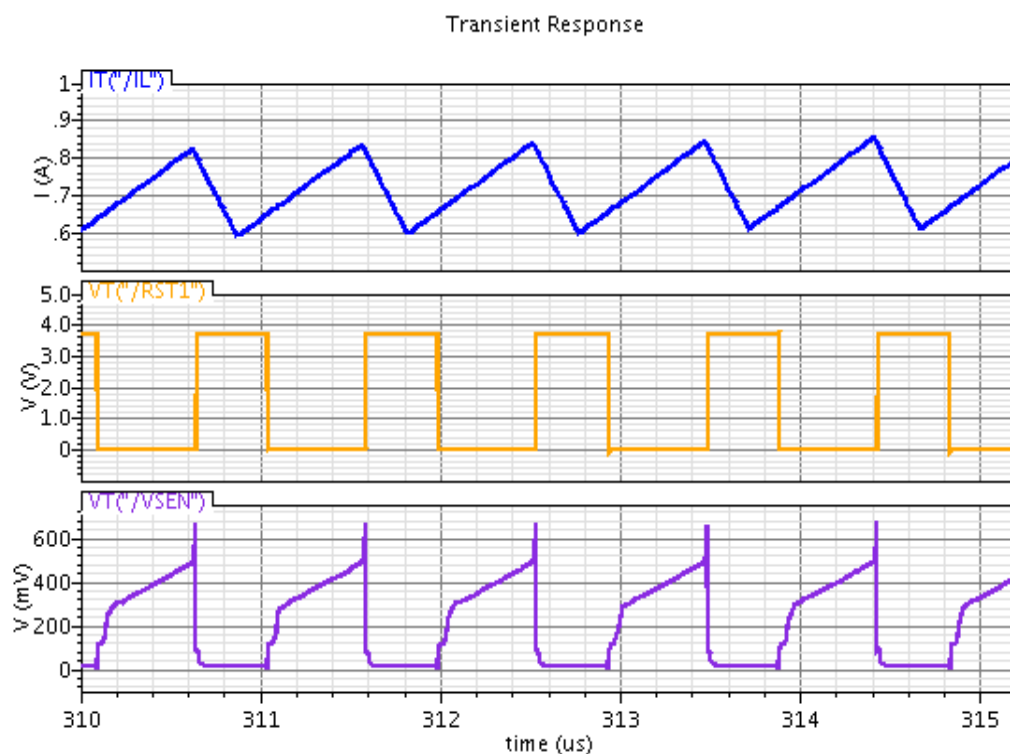


Figure 6. Simulation graph of current sampling circuit.

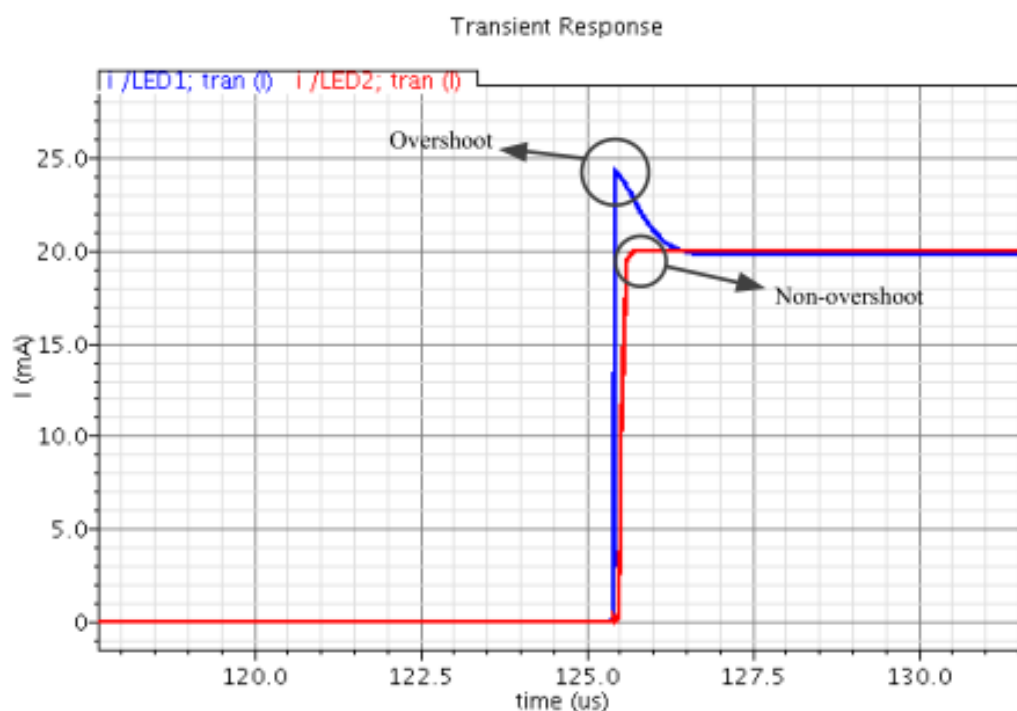


Figure 7. The waveform contrast of the traditional and the proposed circuit.

Figure 7 shows the proposed PWM dimming circuit and the traditional PWM dimming structure of the waveform. Compared with the traditional direct PWM dimming, when the dimming signal is high in PWM dimming circuit, the MOSFET controlled by LDO is the state that transform from cut-off to steady state, rather than the traditional

structure as from the complete guide pass state to the stable working state transition, so there is no instantaneous conduction from VOUT to GND direct path, which effectively avoid the dimming current overshoot of the LED problems.

LED current rise and fall time waveform is shown in Figure 8. It can be seen from the amplified waveform that the rise time in LED current is about 192ns in the LED dimming circuit, and the fall time is about 14ns, therefore the largest dimming can be up to 9000: 1. The reason why current rise time in the circuit is much greater than the falling time is mainly due to when LED is shut down,

HVMOS will discharged through GND, but during the rising time, the response time will be slow, if the rising time is needed to enhance , a proper driver ability design and regulate the CG in HVMOS can be achieved. Finally, Figure 9 shows the system efficiency of the chip at different supply voltages.

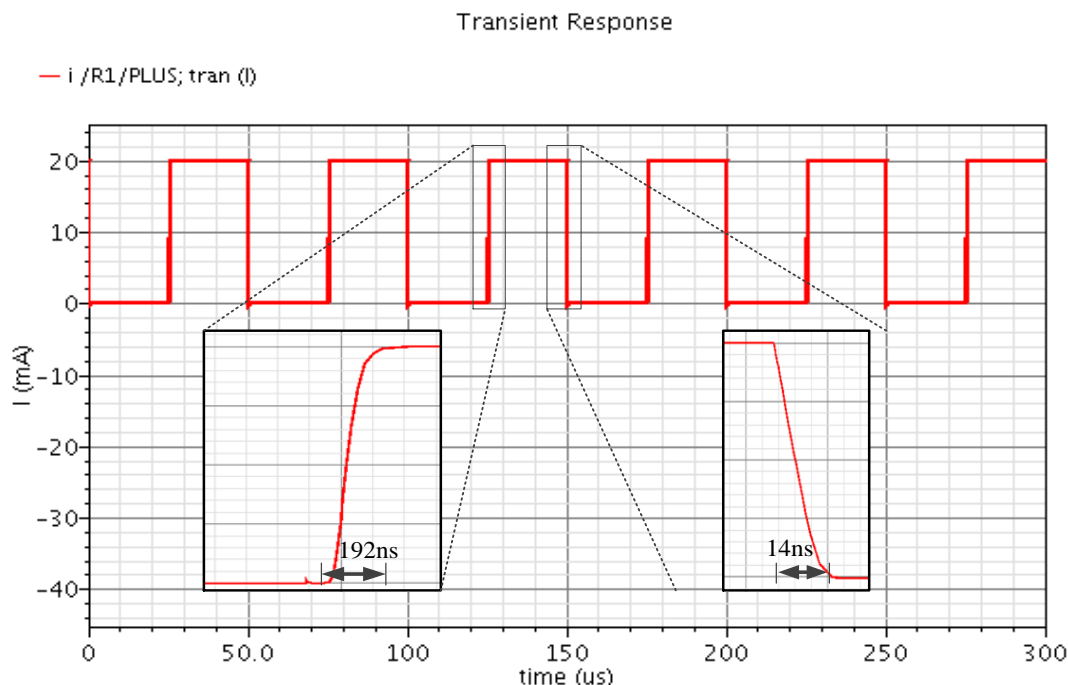


Figure 8. Rising and fall time waveform of the proposed circuit.

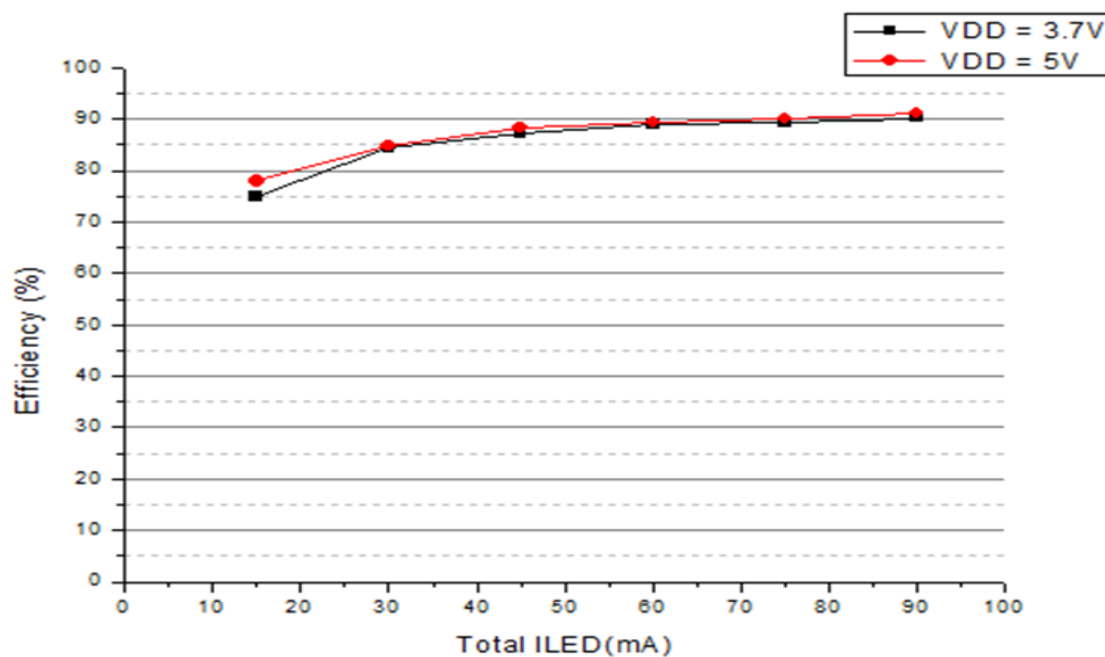


Figure 9. Chip efficiency curves at different supply voltages.

At last, some significant parameters of this circuit and the comparison with other literature parameters are summarized in Table 1.

TABLE I. SIGNIFICANT PARAMETERS OF THE CIRCUIT.

Parameter	This work	[4]	[5]	[6]
Process	0.25 μ m BCD	0.35 μ m 50V CMOS	0.5 μ m BCD	0.5 μ m BCD
Power supply voltage(V)	2.7-5	10-40	3-5.5	5
Output voltage(V)	7-36	N/A	25	2-40
Topology	Boost	Buck	Buck-boost	Boost
External inductor	10 μ H	39 μ H	2.2 μ H	N/A
Peak efficiency	91.4%	92.5%	90.7%	N/A
Dimming ratio	9000:1 @fpwm=500Hz	5:1 @fpwm=10kHz	N/A	5000:1 @fpwm=500Hz

IV. CONCLUSION

A high efficiency LED backlight driver chip for large-screen mobile phone is designed in this paper. A power transistor on-resistance sampling structure is used in the circuit to lower the consumption. A PWM dimming circuit with LDO MOSFET is also used to further enhance the efficiency of the chip. Based on CSMC 0.25 μ m BCD process, spetre simulator is used to complete the simulation and verification. Results show that the maximum dimming ratio can be up to 9000:1, the final output efficiency of the chip can be 91.4% at 500Hz dimming signal.

REFERENCES

- [1] Fei Xu, Lenian He, A High Efficiency Step-up WLED Driver With Wide Range PWM Dimming, 2012 International Conference on Advances in Mechanics Engineering, pp.884-887, Aug. (2012)
- [2] Cheung Fai Lee, P. K. T. Mok, A Monolithic Current-Mode CMOS DC-DC Converter With On-Chip Current-Sensing Technique, IEEE Journal of Solid-State Circuits, Volume: 39, Pages: 3 - 14.(2004)
- [3] Hyun-A Ahn, Seong-Kwan Hong, Oh-Kyong Kwon, A Fast Switching Current Regulator Using Slewing Time Reduction Method for High Dimming Ratio of LED Backlight Drivers, IEEE Transactions on Circuits and Systems II: Express Briefs, Volume: 63, Issue: 11, Pages: 1014 – 1018 (2016)
- [4] Dongkyung Park, Zhidong Liu, Hoi Lee, A 40 V 10 W 93%-Efficiency Current-Accuracy-Enhanced Dimmable LED Driver With Adaptive Timing Difference Compensation for Solid-State Lighting Applications, IEEE Journal of Solid-State Circuits, Year: 2014, Volume: 49, Issue: 8, Pages: 1848 - 1860 (2014)
- [5] SachinRao, Qadeer Khan, Sarvesh Bang, Damian Swank, A 1.2A Buck-Boost LED Driver with 13% Efficiency Improvement Using Error-Averaged SenseFET-Based Current Sensing, IEEE International Solid-State Circuits Conference: 238 – 240(2011)
- [6] J.-S. Kim et al., A fast-switching current-pulse driver for LED backlight, in Proc. IEEE ISCAS, May. pp. 1775–1778(2009)