Methodological Research on Design for Testability of Mixed-signal IC

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Abstract—**The concept and classification of design for testability about IC are introduced. As an example, several testability methods for mixed-signal IC sx1701 are given, which include precise module division, effective control signal building and testing structure adding. By using these methods, the testability of sx1701 is good, and it shows that these testability methods are effective.**

Keywords-design for testability; mixed-signal IC; module division; test control signal; additional test structure

I. INTRODUCTION

Large-scale integrated circuits are usually Mixed-signal IC now, where the digital part usually contains a variety of controllers, memory, timers and registers, through the internal data / control bus for information exchange; analog part usually contains a variety of analog Sub-module. It must be considered that how to make the various parts of the integrated circuit be controlled and observed by the outside world, thereby the test time or test pattern generation time are shortened, and makes it impossible to detect the fault which can be tested and so on in the design phase. That is design for testability issues.

IC testability is considered as a design goal in the initial stage of design which is called design for testability. With the development of integrated circuits, the research on design for testability has made great progress. Therefore, many design for testability methods are proposed. According to the starting point of solving the problem, it is generally divided into targeted design for testability method and general design for testability method.

Some special testability methods for one specific circuit presented by the design which is called targeted design for testability. The advantage of this method is able to lower the additional cost to obtain a higher testability, but there are some shortcomings, for example lacking of regularity, it is difficult to achieve automatic design, and the designer's experience has a higher demand. The so-called versatility testability design method refers to those who fundamentally change the structure of the circuit that uses a number of standard structures and design rules to improve the testability of the circuit, such as scanning path method, boundary scan test technology.

In this paper, a large-scale Mixed-signal IC SX1701 is considered as an example, focusing on the design of targeted testability. For such a large-scale integrated circuit based on the internal controller, the general principle of the controller's design for testability must be followed, that is, the instruction can be input from the outside; the program memory contents can be read out. The timing status signal of the internal controller Can be observed and the functional modules are properly separated from the core control module, which can be directly tested, etc. In addition, ultra-large-scale Mixed-signal test design also has its own characteristics.

II. MODULE PARTITIONING ACCURATELY AND TEST PATTERN GENERATION EXHAUSTIVELY

The most basic design for testability principle is to increase the controllability and observability of the internal module by circuit division, that is to say, a "large" circuit is divided into many small modules by some additional selection logic in the chip test. The different stages of the test signal were selected by the various small modules, thereby improving the testability of the circuit. The use of bus structure is an effective way to achieve the circuit division, shown in Figure 1 SX1701 functional block diagram can be clearly seen that the overall can be divided into two parts of digital and analog. The digital part is divided into modules such as the central controller, the arithmetic unit, the program memory, the data memory, the system register, the timer and the peripheral control, and is connected with each other through the address bus and the data bus. In the analog module, the analog part is usually included the power-on reset, oscillator, voltage detection and a variety of timing generation circuit which make Chip be used to work properly ; also includes the sound or display output, as well as keyboards or other IO interfaces that communicate with peripherals. For such a circuit division, the testability of the circuit can be significantly improved.
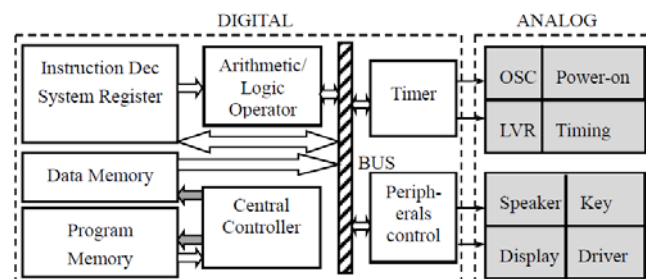

FIGURE I. FUNCTIONAL BLOCK DIAGRAM OF SX1701

For a circuit with multiple inputs and outputs, if any of the output variables of the circuit are related only to a portion of the input variable, then we can divide it into several subcircuits and exhaustively separate these subcircuits Testing, thus completing the entire circuit test, making it possible to test complex multivariable circuits. When testing the circuit with the exhaustive test pattern generation method, the test excitation generator can be a shift register with feedback.

III. EFFECTIVE CONTROLLABLE SIGNAL BE CREATED

Another way to improve the design for testability is to creating some effective control signals in the circuit, such as the set / reset of the flip-flop, some important feedback lines, etc., which can make the state of the circuit controllable and observable, In this regard, in the design of the SX1701 considered a lot.

A. Enter Test Status

SX1701 haven't separated test control pin, and the test status is decided by the input RESET pin state when the IC is power-on, as shown in Figure 2.
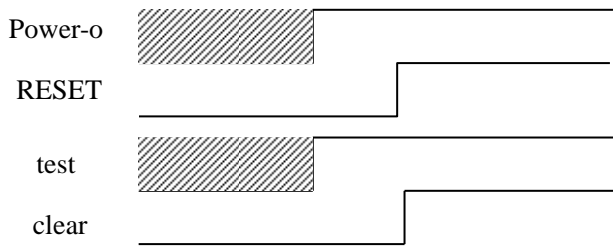

FIGURE II. TIMING DIAGRAM OF TEST STATE ENTERING FOR SX1701

In Figure 2, "test" is test state control signal. When the IC is power-on , if RESET=0, then test=1, the circuit is in the test state; If RESET=1, then test=0, the circuit is in normal working condition. "clear"is system reset signal, power or RESET=0, clear=1, the system is reset in the state, usually clear=0, the circuit is working properly.

B. Internal Test Control Signal is Generating

When SX1701 is in the test state, the configuration of server testing control signal within IC is controlled by the external input pin K0 ~ K3, as shown in Table 1.

IO160 ~ IO165 of the table is the internal test state control signals. These signals used to control the circuit in the test state of the operation.

TABLE I. INTERNAL TEST CONTROL SIGNAL STATUS TABLE

Input pins				Test control signal within IC					
K3	K2	K1	K0	Io160	Io161	Io162	Io163	Io164	Io165
0	0	0	0	0	1	1	0	0	1
0	0	0	1	0	1	1	0	1	1
- - - - - - - - - -				- - - - - - - - - - - -					
1	1	1	0	0	1	1	0	1	1
1	1	1	1	1	1	1	0	0	0
Working States			0	1	1	0	0	0	

C. The Test Timing Signals Generating by the Test Control Signal Internal

The first function of the internal test controllable signal generated above is used to control the generation of test timing signals that directly control the external input of the instruction; ROM content and output detection of the PC contents.

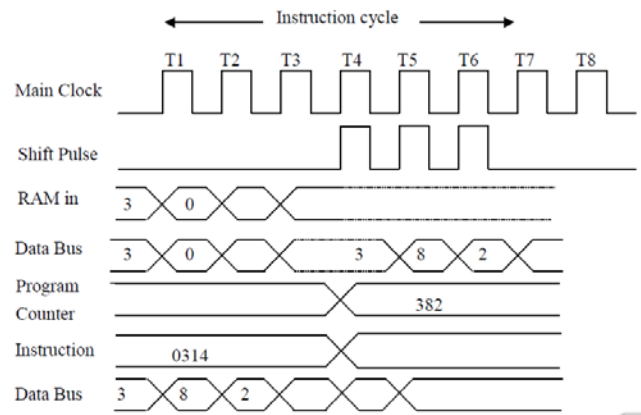With these control signals, IC test can be carried out, Figure 3 is the simulation waveform.

FIGURE III. TEST SIMULATION WAVEFORM OF SX1701

In the T1 period, writing RAM data RAMin can be output from the parallel output pin, because most of the SX1701 instruction execution results are sent to the RAM, so this beat can be used to check the results of each instruction; In T2~T4 periods, the contents of the program counter PC are read from the parallel output port three times under the action of the shift pulse signal. In the T5~T8 periods, the instruction is divided into four times (the first high and the lower) from the parallel output to the ROM output shift Register; In addition, under the action of these control signals, the contents of the ROM can also be output from the parallel port.

D. The External Signal Controlled by the Internal Test Control Signals

The second function of the internal test control signal is to control the input of external signals including the test timing master clock, the controller master clock, the controller timing signal generation control signal, the counter strobe pulse clock input, and so on. The role of these external input signals is to reverse the state of the test part of the circuit, but also speed up the test.

E. The Key Signals Output Controlled by the Internal Test Control Signals

As mentioned earlier, in order to improve the testability, we often know some of the circuit within the key signal state, so these signals should be output, such as the internal controller timing signal; timer main clock signal; crystal vibration control signal; Frequency converter/reference divider output, etc., this part of the function is generated by the above internal test control signal to achieve.

IV. TEST STRUCTURE INSERTING

For Mixed-signal circuits SX1701, the test content typically includes functional testing and performance testing. Functional testing is mainly through the internal digital signal test to determine the function of the circuit whether it is very correct; and performance testing mainly through the internal analog signal test to verify the performance of the circuit. To achieve the above purpose, you must add some test structure in the circuit, so SX1701 part of the circuit is designed for easy testing. The part of the circuit in the normal work does not work in the test state to work.

Specifically, the test structure shown in Figure 4 is added to the SX1701, where the digital signal and the analog signal are selected by a data selector and then output to the test pad.
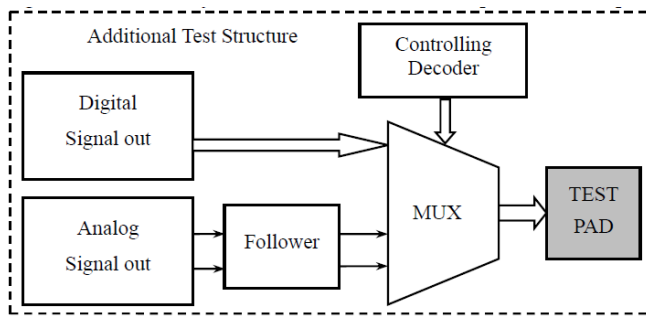
FIGURE IV. ADDITIONAL TEST STRUCTURES IN SX1701

The data selector control signal in Figure 4 can be generated by the test controlling decoder; and the analog signal needs to go through a follower before the data selection, mainly to remove the interference signal, and increase the drive capability. Follower design process needs to focus on the input voltage within a certain range of the signal can follow the output.

V. SUMMARY

More and more methods of design for testability are used in the integrated circuit when IC integration and complexity are improved continuously. Some testability methods for mixed-signal IC SX1701 are given in detail from the perspective of circuit designers. The chip testability and fault coverage have been improved by using these methods.

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