

Design And Research Of A High Precision Σ - Δ A/D Converter

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Abstract

A high-precision Σ - Δ analog-to-digital converter is designed in this paper in order to meet the accuracy requirement of analog to digital signal conversion in the area of high-frequency and low-voltage seismic wave. In the analog part, a second-order Σ - Δ modulator is used to realize oversampling and noise shaping, which greatly weakens the quantization noise. And the digital part of the design was composed by multi-level digital decimation filters including multi-stage CIC extraction filter, FIR half-band filter and IIR high-pass filter to achieve filtering and down sampling function. The combination of two parts finally realizes a low-bit quantitative, high resolution, high signal-to-noise ratio Σ - Δ A/D converter which can output 1 KHz, 24 bit resolution data.

1 Introduction

As computer and communication technology rapidly develop, digitalization in global hi-tech field has been constantly deepening, technology of digital signal processing has been increasingly mature and nowadays, digital technology has become a mainstream in electronic industry. Digital signal system has better stability and higher anti-jamming capacity than analog signal system; it is convenient in transmission, storage and computer processing and it has high precision, low cost and other advantages. Majority of physical signals in nature are not accessible to high-precision observation, comparison, processing, computation, etc. Therefore, it is necessary to convert analog signals to digital signals and process them by digital system to get data desired. The equipment that completes such a conversion is analog-to-digital (A/D) converter. Traditional A/D converter is generally Nyquist rate converter, primarily

composed by analog circuit. Components and parts directly determine the precision that a converter is able to attain. However, as integration is increasingly higher and power voltage is increasingly lower, it is increasingly harder to design a pure analog integrated circuit. Meanwhile, greater demand is placed on signal processing system. In order to meet the demand and make the best of advantages of high speed and integration of modern VLSI, oversampling Σ - Δ (Sigma-Delta) modulation technology is widely applied to A/D convert. Σ - Δ is good for: first of all, its sampling frequency is very high so as to reduce demand for anti-alias filter and greatly simplify circuit. In this way general RC filter is able to meet the demand ^[1]; secondly, Σ - Δ is not required of sample hold circuit; thirdly, the precision of Σ - Δ is generally realized by digital filter, thus it is not demanding on quantizer in the converter and requirements for scale of analog circuit and device match are greatly reduced; fourthly, its negative feedback structure reduces sensitivity of circuit to noise and nonlinear factors and circuit structure is simple. In this paper, the algorithm-level designed on one 1KHz Σ - Δ A/D converter capable of realizing 24 bit high-precision analog-to-digital conversion is completed. Second-order Σ - Δ modulator is applied in analog section and multi-level digital interpolation and decimation filter is applied in digital section.

2 Principle and structure of Σ - Δ A/D converter

Σ - Δ A/D converter or oversampling A/D converter refers to A/D converter whose sampling frequency is far higher than Nyquist rate ^[2]. The ratio between its sampling frequency and Nyquist rate is taken as oversampling rate M of A/D converter. Different from general A/D converters, Σ - Δ A/D converter makes quantizing and coding by difference between the previous value of quantity and subsequent value of quantity or the so-called increment (such a way is called

delta modulation) instead of making quantizing and coding by each sample value in sampling data. In this paper, the idea of Σ - Δ A/D conversion is applied, according to which, the input analog A is made to pass anti-alias filter, alias frequency component is reduced to be as insignificant as possible, signals are made to pass Σ - Δ modulator and analog is converted to a 1-bit digital quantity for output [3,4]. On that occasion, the output intermediate digital quantity is blended with quantizing noise and distortion error resulting from nonlinear element in the analog circuit Σ - Δ modulator. It is then made to pass multi-level digital decimation filter to filter majority of high-frequency noise and make downsampling to Nyquist rate to ultimately output n-bit digital quantity D in higher precision and complete analog-to-digital conversion[5]. Σ - Δ A/D converter is generally divided to two sections: analog and digital. Its analog section is primarily composed by smaller analog Σ - Δ modulator while its digital section is primarily composed by sophisticated multi-level digital decimation filter. Its simple structure is shown in fig 1:

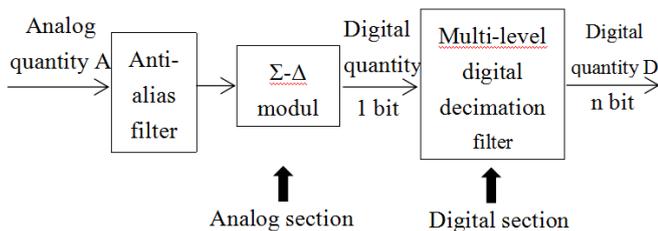


fig.1: Schematic Diagram for Structure of Σ - Δ A/D Converter

3 Second-order Σ - Δ modulator

Quantizing noise is a predominant cause for influencing precision of A/D converter. However, demand of Σ - Δ A/D converter for result precision is not met by oversampling technology applied only or increasing sampling number only. In order to reduce effects of quantizing noise on results, noise shaping principle is introduced to overcome technical difficulty resulting from high sampling by feedback, make periodic extension on sampling signals, and give up sampling time to enhance result precision. Ultimately, total noise power is not changed but noise distribution changes: noise in the low-frequency band will be greatly reduced and

quantizing noise is mostly pushed to higher frequency band [6]. Noise in high-frequency band is better filtered by just adding low-pass digital filter to modulator. Quantizing noise in higher order may be supplied by applying more procedures of integration and summation in the Σ - Δ modulator. According to its modulation principle, the higher order a modulator is in, the smaller error quantizing noise and nonlinear distortion will result in, as a result, the higher precision its digital quantity got will be. Whereas, the higher order it is, the more complicated its circuit structure will be, the harder it will be realized and as a result, its debugging will be much harder. In order to give consideration to both high result precision and circuit simplification, in this paper, second-order Σ - Δ modulator is applied to design analog circuit [7,8] and get the schematic diagram for structure shown in fig.2 by a series of summation, delay, D/A conversion and other operations.

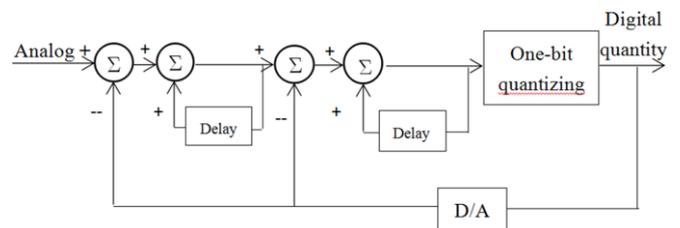


fig.2: Schematic Diagram for Structure of Second-order Σ - Δ Modulator

4 Multi-level digital interpolation and decimation filter

Σ - Δ A/D converter applies an ultra-low-bit quantizer (1 bit), facilitating realization of semiconductor technology; meanwhile, it applies ultra-high sampling rate and Σ - Δ modulation technology to get an ultra-high resolution. Σ - Δ sampling circuit is composed by RC filter circuit, Σ - Δ modulator, photoelectric coupler, digital filter, etc. Since front modulator in the Σ - Δ A/D converter moves quantizing noise to high-frequency band by oversampling technology, its rear digital decimation filter is required to filter high-frequency noise. Therefore, the performance of digital decimation filter plays a very important role in the whole Σ - Δ A/D converter [9].

The Σ - Δ modulator in this design outputs bit stream in 1 bit, 512 KHz. Two points should be taken into account in design of multi-level interpolation filter: on one hand, pass bandwidth F_c in filter of each level should be higher than

signal bandwidth; on the other hand, its transition band should be variable, depending upon decimation multiple of each level. In other words, the cut-off frequency of transition band F_a should be lower than half of output sampling rate in the level. In this paper, multi-level digital interpolation and decimation filter is applied to design circuit in the digital section. The filter is generally graded to three levels including multi-level CIC filter module, FIR half-band filter module and IIR high-pass filter module. Its structure is shown in fig.3. After filter decimation, data of 24 bit, 1 KHz are output. Its cascade mode is designed to be multi-level decimation gradation by reference to CS5378 chip data.

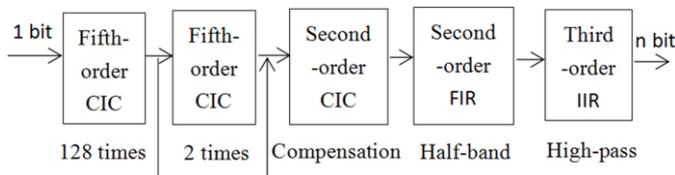


fig.3: Multi-level Interpolation and Decimation Digital Filter

Clock signals offer time control for the whole digital decimation filter system. However, CLK input requirements for each level of filter are different, requiring frequency-division processing in the input clock. On that occasion, PLL (phase locked loop) in FPGA and counting frequency division are applied to realize frequency division. Its principle is shown in fig.4. The voltage-controlled oscillator outputs output signal f_o in tunable frequency which, and input signal f_i/N following frequency division compare with each other for many times and basically equal each other to complete the process of frequency division. Clock input of 2 CIC decimation filters and CIC compensating filter are generated by PLL and clocks of half-band filter and IIR filter are generated by internal frequency-division program.

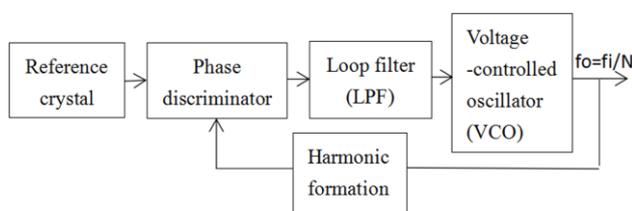


fig.4: Schematic Diagram for Frequency-division PLL

4.1 Multi-level CIC decimation filter

The first level mostly applies a special FIR filter—CIC (cascaded integrator-comb) filter. It is an integral coefficient filter, which requires no circuit in coefficient storage, thus substantially reducing storage units. In addition, it can also save resources and reduce power consumption^[10,11]. In the first level, where input sampling rate and decimation ratio are assumed to be F_s and M_1 respectively, corresponding output sampling rate will be:

$$F_1 = F_s / M_1 \quad (1)$$

The base-band frequency spectrum of output signals in the Σ - Δ /D converter should be rigorously equal to frequency spectrum of input analog signals. In order to protect base-band signals from being aliased in decimation, it is only necessary to filter those signals which may be aliased in the frequency band. If transition band in the filter is deemed as a protected frequency band, the transition band will be left for the subsequent filter processing. In this way, stop band will narrow and frequency-spectrum density of quantizing noise following filter decimation in the CIC (cascaded integrator-comb) filter will keep its pre-decimation form. In other words, frequency-spectrum characteristics of quantizing noise shaping of original Σ - Δ modulator will be maintained. However, sampling intervals increase N times and equivalent quantizing steps decrease N times. Assuming that N is integral power of 2 or $N=2^M$, its resolution will equivalently change from 1 bit input to M bit following filter decimation. While increasing its stop band attenuation, multi-level CIC (cascaded integrator-comb) filter also gives rise to monotone attenuation of signals in pass band. And as cascade level of CIC filter rises, attenuation of pass band will rise by index. Pass band attenuation and stop band attenuation in the CIC filter are contradictory to each other, which is determined by characteristics of CIC filter. In order to meet the demand of Σ - Δ modulator in which filter order in the decimation of subsequent levels is higher than its modulating order, the order of CIC filter in the first level is determined to be fifth-order in this paper. Therefore, pass band and stop band attenuation of CIC decimation filter of first levels are certain^[12]. In filter decimation of the CIC

filter, attenuation of pass band fails to meet the system's demand. Thus, in order to offset roll-off of pass band in the CIC filter, it is necessary to design incremental compensating filter behind the multi-level CIC filter so as to meet the index demand in decimation filter design.

1 bit Σ - Δ -bit stream output from Σ - Δ modulator is input in the digital decimation filter. First of all, the first-level CIC completes 128-multiple decimation of bit stream and the second-level CIC completes 2-multiple decimation. The second-level CIC filter is optional. Gate is controlled based on frequency of data stream. While final output is low-frequency sampling, the second-level CIC filter is gated. However, it is known from the above analysis that CIC filter has certain roll-off attenuation in the pass band, thus it is required to be compensated for enabling output signals to attain design demand. Generally, compensating filter is realized by incremental FIR filter. In this paper, compensating filter not only compensates pass band attenuation but also realizes two-multiple downsampling. On that occasion, one half-band filter is spared. CIC compensating filter is an FIR filter designed in distributed algorithm in essence, which is commonly combined with CIC filter in the variable sampling rate system in application. The fifth-order CIC compensating filter is placed behind CIC filter in this paper.

4.2 FIR half-band filter

The FIR half-band filter applied in the second level is a special 2-multiple decimation or differential value filter, which is more applied in variable sampling rate digital signal processing. As a special linear phase filter, nearly half of coefficients of half-band filter are as accurate as zero. Therefore, operand for filter realization is reduced by nearly a half compared with other linear filters in the same length. In mathematical language, it is signified to be: assuming that transfer function of I-typed FIR filter meets the formula:

$$H(e^{jw}) + H(e^{j(\pi-w)}) \quad (2)$$

Such an FIR filter will be called a half-band filter.

According to the above frequency characteristic and advantage of small operand of the half-band filter, it is applied as a decimation filter whose conversion factor is 2, particularly applied as decimation filter in first levels in

multi-level decimation. Digital signals are required to undergo 2-multiple downsampling after passing CIC decimation filter and compensating filter. This part is realized by half-band filter designed in the equivalent ripple wave method. Half band is a symmetrical I-typed phase FIR filter, whose impulse response of even number is 0. After sampling rate of frequency response in signals declines by half, pass band is at least protected from being aliased in spite of aliasing in the transition band. The intermediate design coefficient is 0.5 and coefficient of other odd items is 0. Due to coefficient symmetry, actual non-zero coefficients account for only 1/4 of total filter coefficients and LE consumption and power consumption are greatly reduced. Besides, due to restricted characteristics of half-band filter, it is not a fit for downsampling in over 2 multiples. Thus, 2-multiple downsampling is most suitable.

4.3 IIR high-pass filter

In the third level, one IIR high-pass filter—third-order Butterworth high-pass filter—is applied, whose frequency response curve in the same frequency band is the flattest of no fluctuations but gradually declining to zero in the stop band. In the poter diagram of logarithmic and diagonal frequency of amplitude, amplitude gradually declines towards negative infinity as angular frequency rises from some boundary frequency on. High-pass cut-off frequency is $0.3\%F_s$ and attenuation rate is 18dB each frequency multiplication, applicable to filtering low-frequency and DC signals. And angular frequency of amplitude of Butterworth filter is in monotonic decrease. The higher filter order is, the faster amplitude attenuation of group frequency band will be.

In the design stage, it is necessary to, first of all, convert given technical indexes of filter to technical indexes of analog low-pass filter on demand; design it to be responding analog low-pass filter based on technical indexes of the analog filter; convert the analog filter to be digital filter in pulse response invariance and bilinearity invariance; and ultimately, get the desired third-order high-pass filter by frequency conversion. Taking existing logical resources in FPGA into full consideration, in this paper, only $0.3\%f_s$ third-order high-pass IIR filter is designed.

5 Simulation and result

5.1 Second-order Σ - Δ modulator

Simulating devices include input signals, voltage followers, integrator in the first level, integrator in the second level, comparators, D triggers, output of the whole modulator, and clock input of FPGA. Besides, signals which the second-order modulator is concerning are primarily high-frequency low-voltage seismic signals. Therefore, many anti-noise peripheral designs are made. Simulation verification is made by socp in the schematic diagram for structure in fig.2.

Since FPGA has no system board in kind, 50KHz square signals transmitted by signal generator are deemed as CLK input in the D trigger. On that occasion, input is made to the Σ - Δ modulator in low level. Waveform output by the whole modulator is as shown in fig.5. The output quasi-pulse “0” and “1” are bit stream desired or 1bit Σ - Δ bit stream.

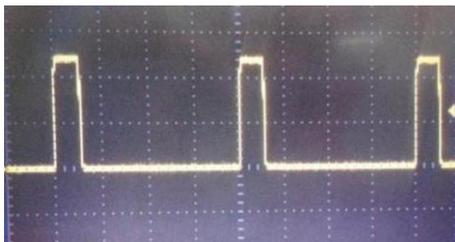


fig. 5: Output Bit Stream Signals of the Whole Σ - Δ Modulator in Low Level Input

5.2 Multi-level digital interpolation and decimation filter

In the section of software design, design and preparation are made by emulating internal information in the chip CS5378. The software Quartus II is applied in preparation and logic analyzer is applied in experiment and revision. The filter is deemed as top to design all filters. Then, they are connected together in order to form an integral digital decimation filter in the principle as shown in the above fig.3, which is not specified any longer. The Σ - Δ modulator outputs 1bit Σ - Δ bit stream which will generate 24 bit digital signals after passing the designed multi-level decimation digital filter.

6 Conclusion

In this paper, A/D converter concerning some specific type of input signals—high-frequency low-voltage seismic signal Σ - Δ A/D converter—is studied. In the section of analog

circuit, second-order Σ - Δ modulator is designed. Oversampling technology and noise shaping technology are applied to change noise distribution frequency band and push it towards higher frequency so as to greatly reduce effects of quantizing noise on results and enhance accuracy of output digital signals. In the section of digital filter, multi-level digital interpolation and decimation filter is applied including multi-level CIC filter module, FIR half-band filter module and IIR high-pass filter module, outputting data in 24 bit, 1KHz after decimating filter. Analog-to-digital combination realizes overall design of Σ - Δ A/D converter in low-bit quantization, high resolution and high signal to noise ratio.

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