Design of 2-Vote-2 Safety Control System Based on FPGA for Railway Train Operation

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Abstract. In the railway system, the speed of trains is increasing continuously. In order to improve safety and reliability of signals, a 2-Vote-2 safety system based on single FPGA chip and multiple IP soft cores is designed. The control system embeds two MC8051 IP cores and a 2-Vote-2 module which is consisted of two 74373, four 74377 and one PLL inside FPGA. Using speed information of the DC motor to simulate train operation state information, the system realizes control of train operation states. The system has high integration, low power consumption and better safety by redundancy of the railway system. The designed 2-Vote-2 comparing unit allows +3% errors for input information, which improves system reliability. Experimental tests validate that the control system is able to control speed of the DC motor. Additionally, experimental results demonstrate the safety system could stop the motor in time and give corresponding alarm information when the operation is illegal.

1. Introduction

With the improvement of science and technology level, the speed of trains is becoming faster and faster, and the transportation capacity is sharply increasing. We pay more attention to the reliability and safety of the railway system. Using redundancy technology to improve the performance of the system is an important research direction of the railway system. Therefore, researching on the improvement of this technology has also become the focus of the railway system in recent years.

At present, most redundancy technology uses more than one hardware CPU to accomplish the same task, so as to ensure the safety and reliability of the system [1]. For example, a typical double 2-Vote-2 structure redundant computer is implemented by two identical subsystems, and each of the subsystems is processed by two identical CPUs implementation logic. Such redundant structure undoubtedly increases the volume, quality and cost of the system, and seriously hinders the rational redundancy of the railway system [2].

2. Overall System Scheme

This design of 2-Vote-2 safety control system consists of CPU module, speed sensor module, isolation module, drive module, keyboard module, display module, power module, alarm module and controlled object, as shown in figure 1.

The CPU module of the system is embedded in the FPGA. Two MC8051 IP cores are embedded into the chip building the 2-Vote-2 safety structure. The CPU modules are the core of the control system. Data inputted by the keyboard module and the speed sensor module are transferred to CPU module. CPU module does data processing and votes for its results, and then it outputs signals to river module, display module and alarm module. Different voltages throughout the system are supplied by power module.

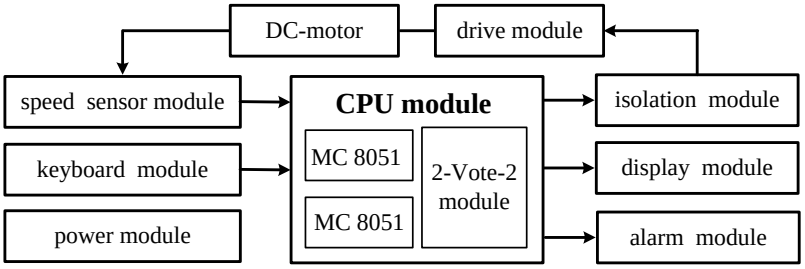

Fig.1 Overall block diagram of the system

3. Design of FPGA Module

In the traditional redundant systems, two hardware CPUs and some other chips are needed to realize the 2-Vote-2 safety control system of railway train operation.

The CPU module in this system uses the EP4CE10F17C8N chip of Altera company, embedded two MC8051 IP cores inside, using two 74373, four 74377 and one PLL macro function modules to form a 2-Vote-2 comparing unit [3]. The two processors collect system input data, process data and output process results independently and synchronously. The 2-Vote-2 comparing unit compares the outputs of the two processors. The operation is valid only when the outputs are the same, in which case the CPU module is considered valid [4, 5]. The connection of the CPU module is illustrated in Figure 2.

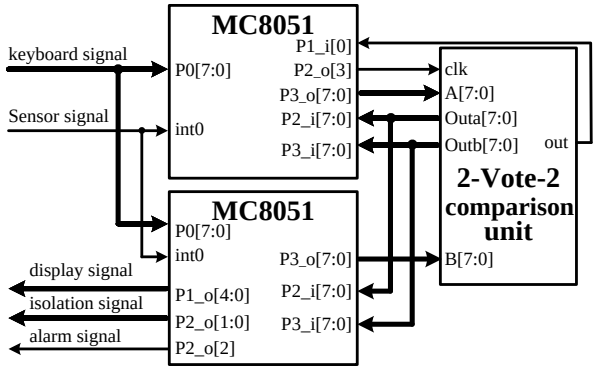

Fig.2 Structure diagram of FPGA module

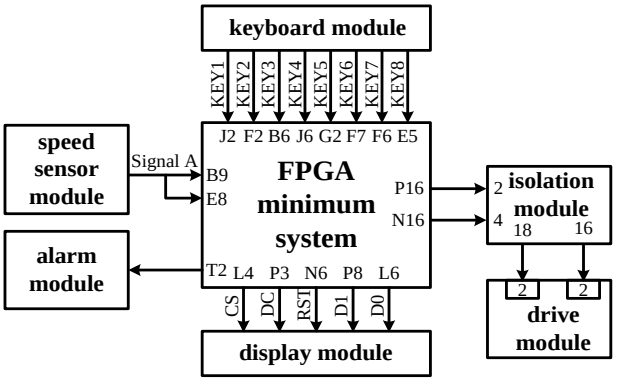

Fig.3 Schematic diagram of other modules in the system

4. Design of Other Functional Module

The schematic diagram of other modules in this system is shown in figure 3.

The speed sensor module adopts mini256z encoder, which is used to convert the speed information of DC motor into electrical signals and pass it to CPU module.

The keyboard module is used to input control information of the system. The keyboard adopts 4*4 matrix keyboards. The keys 1-10 are numbers 1-9 and 0. The key 13/14 is an acceleration / deceleration button whose step is 10. The key 15 is a reverse button. The key 16 is a start button.

The display module approves OLED (Organic Light-Emitting Diode), and the SPI interface, which can be used to display the input data and the operation state of the system.

The isolation module adopts the 74LS244 chip, which is used to separate DC motor from control module, and reduces the interference of DC motor. Meanwhile, the large current of the motor is avoided to burn out the control chip in this way.

The driver module is made up of two BTN7970 chips. Each BTN7970 chip is a half bridge circuit. Two BTN7970 chips form an H bridge circuit to realize the control of the rotation speed and the steering of DC motor.

The alarm module uses the buzzer circuit, which is used to give a false alarm when the system operation is illegal.

5. Design of System Software

5.1 Main Program

The main program of this design is a circulation. The main design idea is setting the initial value of the MC8051 output duty cycle firstly, and then adjusting the output duty cycle according to the system requirements. Thus, the speed and the steering of the motor are controlled. The overall flow of the design is presented in figure 4. The system software consists of a main program and several subprograms. The main program is that MC8051 scans keyboard module, and then sets the speed of the system according to the keyboard input information. The MC8051 compares the set speed information with the actual speed information detected by the sensor, and then adjusts the PWM output duty cycle. Thus, the motor is controlled to achieve a preset speed value.

5.2 PWM Speed Control

This design controls motor speed regulation by a subprogram. The MC8051 adjusts the PWM pulse width by modifying the duration of the pulse. Thus, it realizes the speed control of the motor. PWM waveform generation process is shown in figure 5.

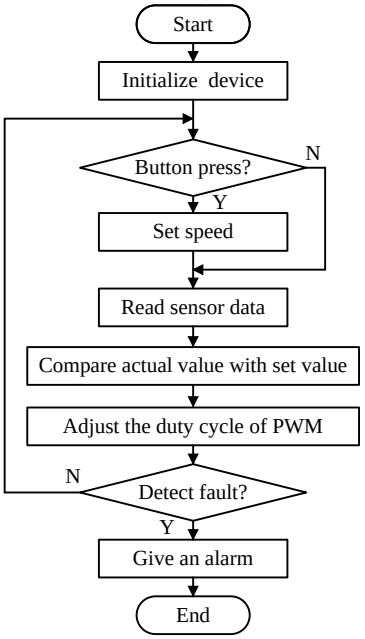

Fig. 4 Overall flow of design

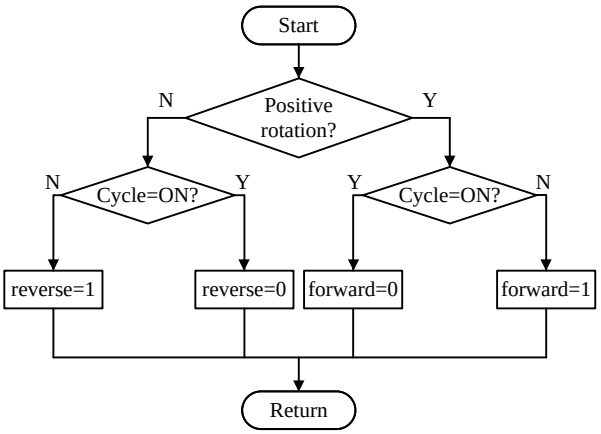

Fig. 5 PWM waveform generation process

6. System Testing

After the completion of system hardware and software, the function of the whole system is tested.

Tests result shows that when the system is operating normally, the output results of two controllers are the same, and the output results of the 2-Vote-2 comparing unit modules are normal. The output waveform of the oscilloscope is illustrated in figure 6. When one of the processor's output waveform fails, the buzzer gives an error alarm indicating that the system is unsafe at this time. When the system is unsafe, the output waveform of the soft cores is shown in figure 7.

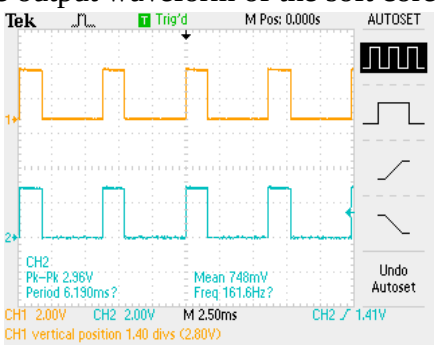

Fig. 6 Waveform when system is working normally

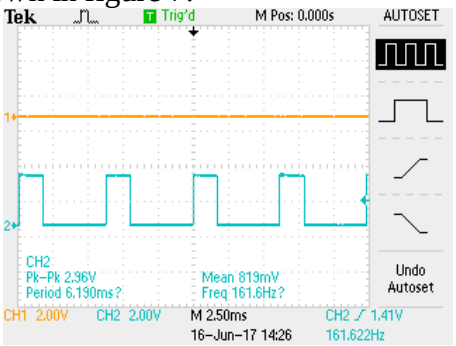

Fig. 7 Waveform when system is unsafe

7. Conclusion

The design implements the idea of embedding multiple MC8051 IP cores into single FPGA chip, which requires two separate processors and multiple external circuits in the past. The system structure could be reconfigurable with high integration. The 2-Vote-2 module increases system safety and reliability by redundancy. Moreover, it is convenient to redesign circuits with low development cost.

Acknowledgements

The corresponding author of this paper is Cairong Zhang.

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