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Design of a Frequency Counter Based on Input Capture Function of a Single Chip Computer

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Abstract. By adopting the single chip computer ATmega16 as the control unit, a frequency counter is designed based on the input capture function of the single chip computer assisted with the appropriate software and hardware resources. This frequency counter can realize real time, high-precision frequency measurement. The results prove that this system can steadily measure the frequency of the sensor, and the measurement error meets the requirements of design.

Introduction

In the field of electronic test, the frequency measurement is one of the most basic measurements. Frequency signal has strong anti-interference ability and higher measurement accuracy. It is easy to be transmitted. Therefore some definite function relations are used to convert the measurement of other electrical parameters into the measurement of frequency signal. In practical applications, the physical parameters such as force, rotation rate, displacement, velocity, flow, etc are generally measured by a digital sensor, and then are converted into pulse signals, and then their frequencies are measured.

The control core of a traditional frequency counter is usually made of a combination circuit and a sequential logic circuit. Its shortcomings include too complex structure, poor stability and lower accuracy[1-9]. When the high measuring accuracy of frequency in the test is required, the frequency counter which is based on the traditional frequency measurement principle is difficult to meet the requirement. Therefore, the problem how to improve the measuring precision is critical. By using the frequency counter designed in this paper which has the input capture function, the measuring precision will be improved. The structure of this frequency counter is simple, and its frequency test has high precision. The designed measuring range is from 10 Hz to 256 KHz, and the frequency magnitude can be observed in real time on the personal computer (PC).

Control core

The main chip uses a low-power consumption 8-bit microcontroller ATmega16 produced by Atmel corporation which has the reduced instruction set computer (RISC) structure. Its single cycle instruction ensures high execution efficiency and low cost, and its high speed processing capacity is up to 1 million instructions per second / MHz. The chip provides 16K bytes in-system programmable (ISP) flash program memory which can be erased more than 10,000 times, 32 programmable Input / Output ports, two 8-bit timing counters, a 16-bit timing counter which has the function of input capture, a programmable serial interface called universal synchronous/asynchronous receiver/transmitter (USART), one serial peripheral interface (supporting in-system programmable program downloading).

Frequency measurement principle

Normal single chip computer uses timing method for frequency measurement. This approach requires two timers, or a timer and an external interrupt, so two hardware resources must be occupied. The first timing counter T/C1 of the ATmega16 single chip microcomputer has an input capture function unit (see Figure 1), which can provide a high accurate measurement of cycle. The function can accurately capture the occurrence of an external event and record the time stamp of event occurrence. By using this function for the measurement of frequency, not only just one hardware resource (namely the timing counter T/C1) is occupied, but also high measurement accuracy can be achieved. ATmega16 is an 8-bit single chip microcomputer, but the T/C1 is a 16-bit counter, which has the characteristics of high precision and wide time range compared with the normal 8-bit counter.

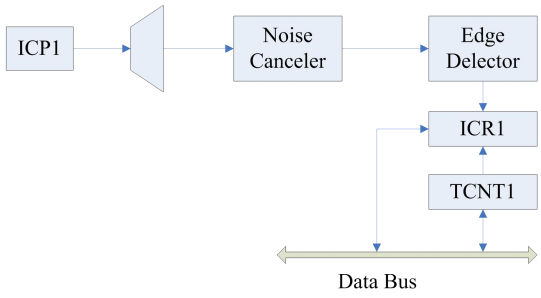

Figure 1.T/C1's input capture function unit

TCCR1B is a control register of the timing counter T/C1. When the seventh flag set ICNC1 is 1, it makes input capture trigger signal of noise canceller. The noise canceller circuit is a digital filter. Only when the four sampling values of the trigger signal are equal, the signal will be triggered. The trigger mode of input capture signal is decided by the set value of the sixth flag ICES1.

When the rising edge trigger the input capture event, namely the logic level of the pin ICP1 changes from low to high, the value in the register TCNT1 of the timing counter T/C1 will be automatically and synchronously replicated into capture register ICR1 by the timing counter hardware. Then the input capture flag ICF1 is set to generate an interrupt request. That is, when the input signal from pin ICP1changes from low to high every time, the count value in register TCNT1 will be synchronously replicated into the capture register ICR1.

If the two consecutive data from the capture register ICR1 are recorded, and then the cycle time of the input signal may be obtained by multiplying the different value between the two consecutive data with the known counting pulse cycle of the counter. In the entire process, the counting action of the counter is not influenced at all, and the time stamp of the capture time is automatically and synchronously replicated into the capture register ICR1 by the hardware, consequently the obtained cycle value is very accurate.

System Design

System hardware design. The system control core is ATmega16, and it is a minimum system which supports the ISP. The system hardware principle is shown in Figure 2.

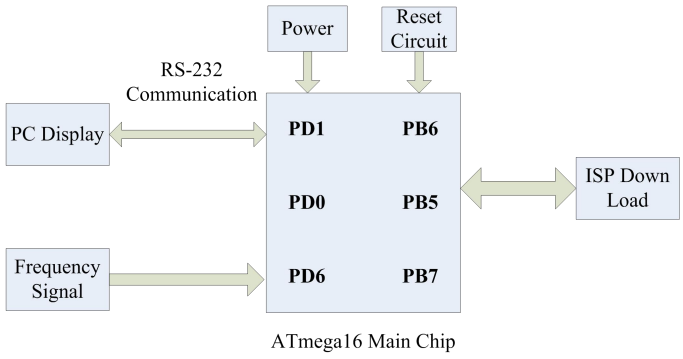

Figure 2.Schematic diagram of the system hardware

Frequency signal is input from capture register ICP1 (namely PD6 as shown in Figure 3). The ATmega16 microcontroller chip provides four kinds of resistance and capacitor (RC) oscillation source, which can be easily used. However, in order to improve the accuracy of the test, the frequency of the system clock is set as 4 MHz, and the cycle is 0.25 μs.

The measuring main circuit of the frequency counter is shown in Figure 3.

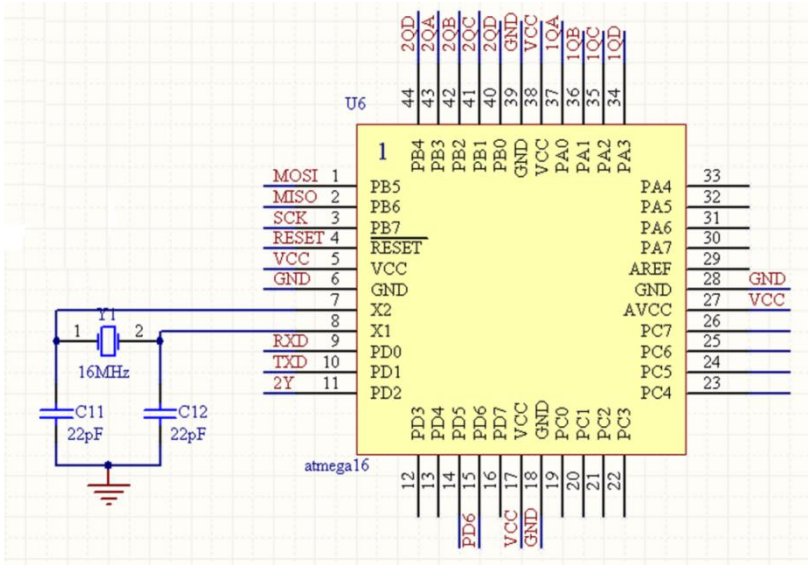

Figure 3. Schematic diagram of main circuit

System software design. The system software mainly includes three parts: initialization phase, frequency measurement phase, and final communication phase. The modularity process can reduce the probability of errors.

Since the frequency range of the measured signal is relatively large, automatic range conversion mode is needed. Determination of the range is constrained by the length of T/C1, the pulse frequency of the counter and the measured frequency. After the initialization in T/C1, two ICR1 values are recorded in the input capture interrupt service of T/C1, one of which is the obtained value when it is triggered 0 time, another is the obtained value when it is triggered 1 time. When the second value is recorded, all interrupts on T/C1 are banned.

In the frequency measurement subroutine, the two ICR1 values of each group should be judged and the difference between them can be obtained by the subtraction, and then it should be decided whether it is overflowing or not. The overflow here means that the second value is greater than the first one, and the value in the register TCNT1 appears from 65536 to 0. Once the overflow occurs, it shows that the difference exceeds the length 65536 of the 16-bit timing counter T/C1. In order to

reduce the lower limit value of the measured frequency, a flag is set to record the number of overflow in the overflow interrupt of the T/C1 for facilitating later calculation of frequency value.

Additionally, in order to estimate the validity of the data, only the measurement data that the two consecutive effective differences are equal can be used as a valid cycle measurement data in the frequency measurement subroutine. Thus data errors resulting from the external disturbance and the untimely interrupt response can be excluded effectively.

It is necessary to judge whether the frequency value is greater than 8 KHz after a measured parameter is converted into a frequency value in order to perform the corresponding range conversion. The reason taking 8 KHz as the boundaries is as following: When the system clock is set to 4 MHz and the record interval is set to 1 which indicates the time lag between two adjacent rise edges, the 500 pulse numbers can be recorded as the timer pulse frequency is 1/8000 s. When the system clock is set to 4 MHz and the record interval is set to 128 which indicates the time lag between 128 adjacent rise edges, the 64000 pulse numbers can be recorded as the timer pulse frequency is 128/8000 s. The pulse numbers of the above cases are all smaller than the length 65536 of the timing counter T/C1. Namely， when the measured frequency is greater than 8 KHz, the range is converted into 128 automatically. Once the frequency is smaller than 8 KHz, or the measured data is overflow, the range is automatically converted into 1.

Data measurement and analysis

The typical measurement data for pulse frequency signal are shown in Table 1. The errors between the measured frequencies and the standard frequencies are very small as can be seen from Table 1. So the design of the frequency counter based on input capture function of a single chip computer can meet the requirements.

Table 1 Typical measurement data for pulse frequency signal

Pulse	500	200	1600	3200
The fist	499	199	1599	3200
The second	499	200	1600	3200
The third	500	200	1599	3200
Average	499	200	1600	3200
Error/%	0.0	0.1	0.01	0.12

Conclusions

A frequency counter based on the input capture function of a single chip computer is designed. It has the higher precise than that of the traditional frequency counter usually made of a combination circuit and a sequential logic circuit for the frequency and cycle measurement. The whole measuring process maintains a high stability and high precision. The circuit structure is simple and easy to realize.

Acknowledgements

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Conflict of interest

None declared.

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