Design of Image Acquisition System Hardware for Placement Machine

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Abstract. Based on the placement machine vision recognition system for functional requirements, this paper proposed a vision system design. Combined with the latest electronic technology and the results of the FPGA, the Nios II system is applied to the placement machine vision systems, and proposed an overall hardware design of FPGA-based machine vision system.

Keywords: The placement machine, FPGA, Nios II system

Introduction

With the application of surface mount components more and more widely, placement machine capable of accurately and efficiently completing placement task has become more and more prominent in the electronic manufacturing industry. However, the current high-end equipment installed is monopolized by the foreign, at present, the research and development of the technology and equipment of the electronic components is still in the initial stage in China, as a guarantee of the precision of the system, the visual system plays a very important role in improving the performance of the placement machine and improving the quality of the system. [1]According to the need for SMT placement of electronic components, angle error factor identification, on the basis of the research and analysis of the development status of the domestic and overseas placement machine and its visual system, we study and develop a new visual recognition system.

Overall design of the system

The hardware design of the system is as follows:

ARM+PC machine: The scheme uses ARM chip for image acquisition, which is the core of the control system of the chip, PC is mainly responsible for image processing, which will have a good advantage in image processing because the operation rate of PC and the algorithm is relatively easy to achieve. But the need for multi machine communication, as the image resolution becomes more and more high, which will become more difficult in the image data transmission, so that the overall rate of the system down, and the system is huge, not easy to carry.

Compared with the above scheme, the scheme has no change, but the system integration is higher, and easy to carry, however, in terms of data processing is far less than the rate of PC machine, Moreover, it will also bring negative effects in the multi machine communication. [2]

From the above two programs, image acquisition and image processing are carried out separately, so there will inevitably involve the case of multi machine communications, then the rate will fall. The biggest feature of FPGA is that it can run in parallel, and can be embedded in the kernel, so this paper uses the FPGA program, namely，image acquisition and processing are in the same chip, which avoids the problem of multi machine communication, and the working rate of FPGA is higher than that of ARM and DSP.

In the overall design of the system, we used EP3C16Q240C8 Altera company's chip as the main control chip to construct the image acquisition and processing system with the HY57V641620 OV7670 digital CMOS image sensor and HYUNGAU the SDRAM memory chip, and display mode used Black DB2C8TFT32 LCD screen, and which upload to the host computer for processing and displaying by serial port mode. The overall block diagram of the system is shown in Figure 1.

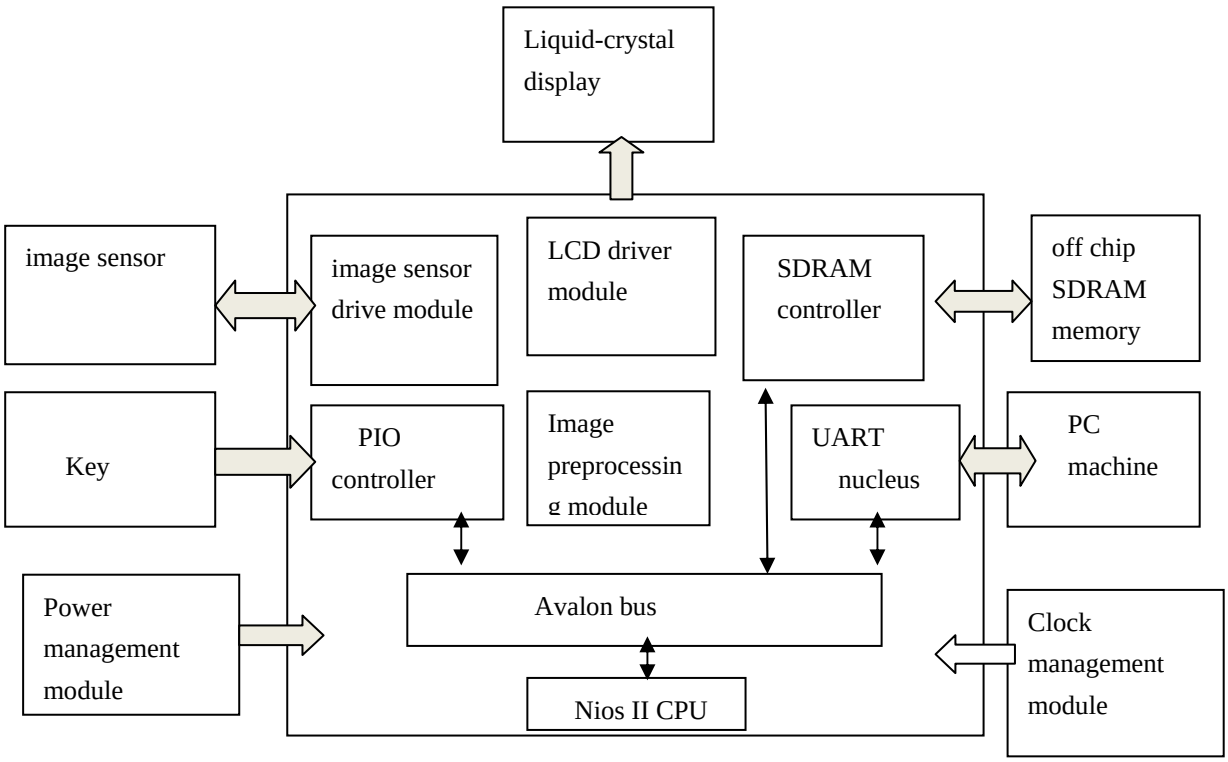

Fig. 1 the overall designer diagram of the system

System working principle

The main function modules of the system are as follows:

Power module: 5V DC power supply, and with the AMS1117 chip to provide 1.5V, 2.5V, 3.3V power supply.

Clock module: FPGA core chip clock is provided by the external and the clock source by a 20MHZ crystal frequency access chip global clock pin. The system clock of the OV7670 image sensor is 25 MHZ, and in its drive the sensor will output a 8 bit data every one cycle along with the line signal and the frame signal.

Image acquisition module: The main function of this module is image information collection and storage. This module provides the driving sequence for the image sensor and controls the image acquisition and output of the image sensor, FPGA accepts image sensor

output data and carries on format conversion, in the end, the image information is stored in the external SDRAM chip.

Image preprocessing module: The main function of this module is Image preprocessing and Implement some basic algorithms, such as image grayscale conversion, filtering, edge detection, histogram equalization, etc.

Image display module: The main function of this module is to display the image collected by the chip.

Storage module: Due to the large amount of data needed to be processed, the program uses 16 two bit SDRAM chip in parallel to form a 32 bit memory module.

Serial transmission: To exchange data or commands with the host computer.

The working process of the system is as follows: After the system starts to run, Firstly, Functional configuration of the sensor by FPGA enables the sensor to work properly as required, when the configuration is complete, the sensor will return the configuration complete signal, and the image is collected and output under the driving sequence. Within the FPGA there are two caches with a dual port ram, at first the first line of the picture is entered into one of the ram, the ram has been written after the end of the first line, then change another ram received data, and under the control of the kernel full RAM send data to the SDRAM storage or directly into the display module; In the preprocessing, the image is read from the SDRAM, which is transformed into a format that facilitates the processing of an image and sent to a preprocessing module for processing. [3]

Image acquisition and storage

In the image acquisition module the OV7670 digital CMOS image sensor is used as the image acquisition device. The sensor not only has small size, but also has a low operating voltage, including all the features provided by the VGA camera. Through the SCCB bus the sensor can be controlled, and some configuration data can be got, such as the whole frame, the size of the window, sub sampling, resolution, and other data. The speed of the VGA image transmitted can reach 30 frames. Users can control the sensor through the SCCB bus, such as the quality of the image, the output of the data grid and transmission mode, etc.

Design of SCCB bus control module

Design principle of SCCB bus controller

Since the start and end of the SCCB sequence is achieved by the level of the data line and the clock line level, and the data is transmitted along the rising edge of the clock line. In order to meet the above requirements, we used the following design method: The clock and data are viewed as a set of output data, which driven by clock qualified signals will be serial output as long as it, and at the output we can get time sequence which meet the requirements of the SCCB bus.

Process in the NiosII kernel: When data is output from the kernel, there need to give the SCCB bus module an output signal load, In the bus module, its performance is the number of signal, the data being put into the cache, when the bus module receives the data, it will return to a busy signal sccb_Full, namely, the kernel is prohibited from continuing to send data to the bus until the module sends out the data and cancels the busy signal.

Design scheme of SCCB bus controller

The interface module of SCCB bus controller is shown in figure 2.

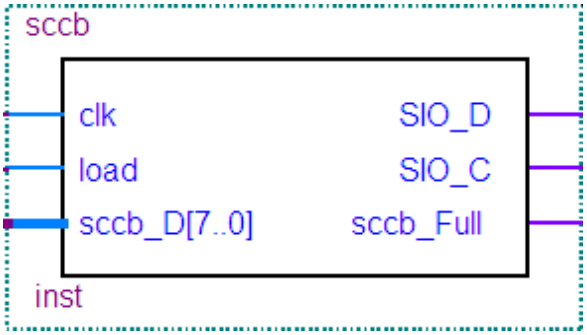

Fig.2 The interface module of SCCB bus controller

SCCB bus controller interface schematic as shown above, CLK is the drive signal of the controller, Load is the signal to send data to the kernel, sccb_Full is busy signal of controller, SIO_D and SIO_C are two sets of data output port, which is driven by the clock CLK, sccb_D[7:0] is the parallel data input port.

Memory cell allocation

In the image acquisition and processing system, in the image acquisition and processing system, due to the need of image displaying and processing, it is necessary to temporarily store a frame of image, There are two methods for caching data generally, one is to use ram resources inside the FPGA chip, and the other is to add external memory devices. In this design a frame of image data needs to occupy 320*240*2=153600 bytes, but EP3C16 chip is only about 500K of storage space, so there are unable to meet requirements of its space, only by ram internal FPGA resources, therefore, this design uses the method for external adding memory chip.

Here we use the SDRAM controller module of NISO2 embedded soft core, which is a good solution to the above problems. SOPC_Builder has integrated the SDRAM controller core, which the user can easily apply to the SOPC system.

Implementation of image acquisition and storage

The main function of image acquisition module is responsible for driving the image, and the image information collected by the sensor is stored in an external SDRAM chip in a certain format[4]. Image acquisition and storage module structure diagram is shown in figure 3.

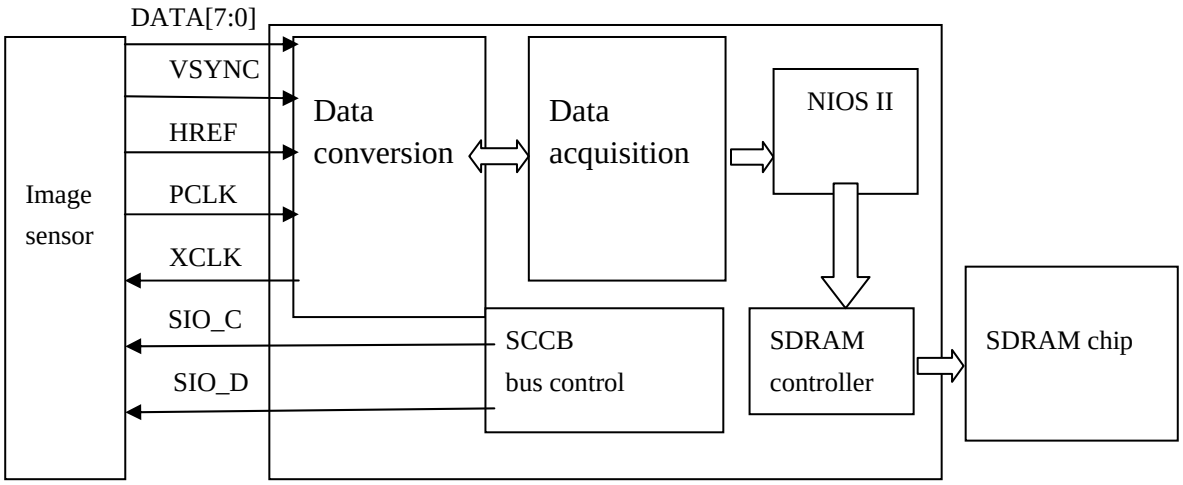

Fig. 3 the structure of image collect and storage module

FPGA drives image sensor OV7670, which configuration process is achieved through the SCCB bus module. SCCB module sends configuration information to the image sensor, including the image output format, the size of the ranks, RGB gain, etc. Image sensor configuration has completed, which returns to the collection of digital image information to FPGA. Because it is the output of digital information, which can be directly input into the FPGA chip, so we do not need to carry on AD conversion.

Display module control unit design

In the display operation, the data that need to display comes from the image acquisition module, rather than the external SDRAM chip. The data collected by the image acquisition module is 16 bits, that is, a pixel data, In the show, we only need to put these data into the LCD memory. At the beginning of the system, the LCD is initialized, which is done by the II Nios kernel. Since the CS pin is needed during initialization, the two clock signals from the NiosII core and the external hardware module are separated from each other in the design so that they can not influence each other. The design method is shown in figure 4.

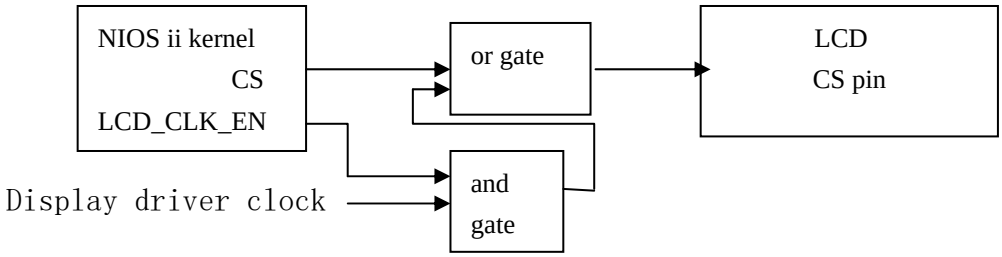

Fig.4 The control method of CS pin

From the figure above, when the LCD is initialized, the pin LCD_CLK_EN is set to 0, then the LCD pin is controlled by the NiosII kernel. When the initialization has completed and data comes in, then NiosII core will CS are set to 0, and the LCD CLK en 1, so the LCD of the CS pin is connected to a display driver on the clock and the data will be written to memory on the falling edge of the clock. In the data acquisition and storage module, the data in the pixel in the role of PCLK get into the dual port RAM. NiosII kernel will be notified

when RAM is full, Then the kernel only need to write the corresponding program to achieve the above process, namely the collected data has been sent into the LCD memory.

Conclusion

In this paper, the hardware design scheme of the image acquisition system is presented, and the collection module, storage module and display module of the program were simulated in time sequence, which results have reached the expected requirements of the design.

Acknowledgments

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