A New Preparation Process of Double-gate FETs Based on Monolayer Graphene Nanoflakes

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Abstract: A new preparation process to product double-gate field effect transistor (DG-FET) of monolayer graphene nanoflakes, fabricated by mechanical exfoliation, was systematically studied in this paper. The graphene DG-FETs are bipolar and possess high gate modulation (On/Off ratio is large), and higher regulation accuracy, which is double-gate regulation. These results showed the extraordinary performance of the double-gate FETs based on monolayer graphene, which might open a new road to develop graphene-based material in the application of double-gate FETs.

Introduction

Since graphene has been discovered by Geim and Novoselov in 2004[1], this two-dimensional (2D) material with typically extraordinary properties has attracted extensive research in the last few years[2-5]. Disappointingly, low On/Off ratio and low regulation accuracy has immensely restricted the application of this star material in logic transistor field and optoelectronics[6,7]. Fortunately, DG-FET is an effective way to solve the problem, which has extraordinary properties. So it is necessary to expand a better path to produce the DG-FET.

Although the concept of DG-FET has been put forward for a long time[9-16], few researchers can stably produce DG-FET. Therefore, a new preparation process of DG-FET based on monolayer graphene is systematically put forward in this paper, which exhibits extraordinary properties[16-20].

Results indicate that the graphene DG-FET, fabricated by the new way, has a larger On/Off ratio and higher regulation accuracy, compared to traditional graphene FETs and graphene DG-FETs are produced by other way. More importantly, we open up a new road to produce monolayer graphene DG-FET stably and normatively. Accordingly, this graphene DG-FET may possibly be more promising in the application of FETs.

Experimental Details

Device fabrication: The DG-FETs based on graphene were fabricated by standard micro-nano technology(EBL, ALD and EBE). The preparation is divided into two parts: back gate preparation and top gate preparation.

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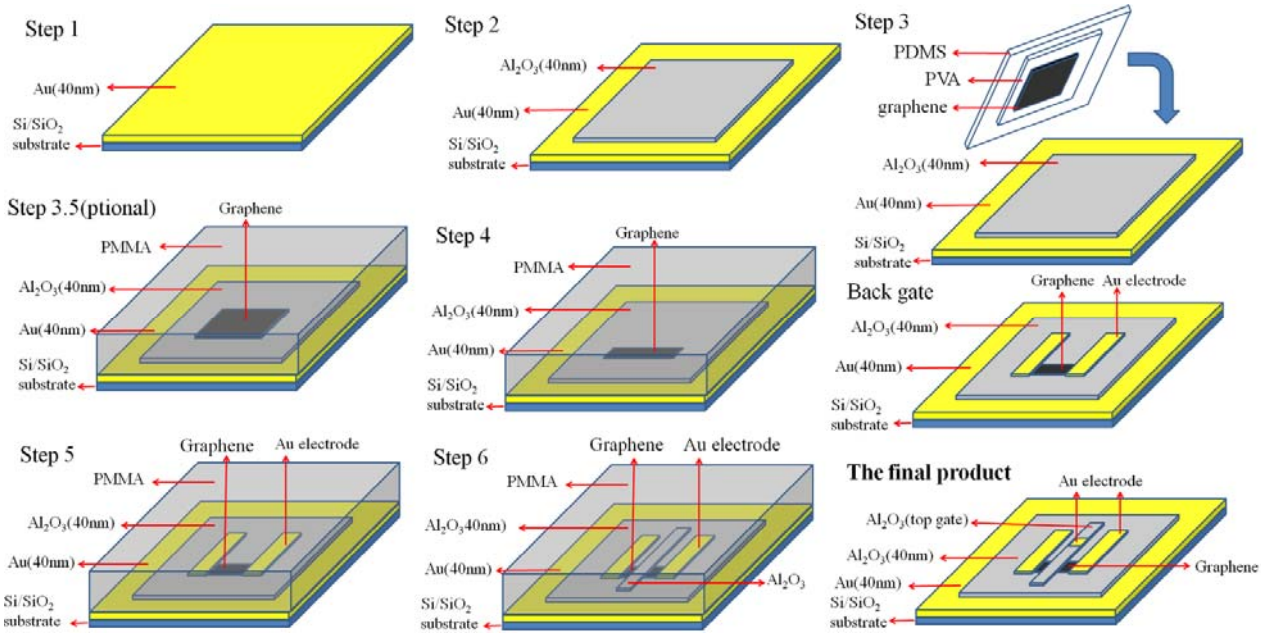

Figure 1. steps of the preparation of DG-FETs which is divided into two parts. (a) four steps of the preparation of back gate.(b)the other two steps of the preparation of top gate and the final DG-FET.

Firstly, The gold is evaporated onto 300 nm Si/SiO_2 (doped p++, conductivity: 0.01–0.02 Ω·cm) substrate About 40 nm which fabricated by EBL(electron beam lithography) and EBE(electron beam evaporation). Secondly, 5 nm of alumina(Al_2O_3) was deposited on the Au film by ALD(atomic layer deposition) with somewhere uncovered. Thirdly, the graphene nanoflakes were exfoliated from the graphite crystals onto 300 nm SiO_2/Si substrates using mechanical exfoliation technique and find suitable monolayer graphene sample under the microscope. Therefore, The graphene sample was transferred onto the Al_2O_3 film by heterojunction fixed point transfering technique. There is a step optional that the monolayer graphene had better be etched away after covered PMMA and lithography if it is irregular in shape after step 3. Fourthly, gold electrode was made on graphene after several step: rotating rubber, EBL, EBE and acetone cleaning. Up to now, back gate preparation, half of all, is completed.

The other parts, preparation of top gate, are of vital importance. Fifthly, Making the shape of top gate by EBL in the sample which covered by PMMA, and covering the shape , fabricated by ALD System, by Al_2O_3. By the way, the Al_2O_3 should not cover the Au electrode. Finally, once again like step 4 to make Au electrode in top gate. Thus, we get the final product double-gate monolayer graphene field effect transistor.

Results and Discussion

Characterization of monolayer graphene nanoflakes and DG-FETs: Firstly, The DG-FETs were characterized by SEM to comprehend the surface photography of Alumina and section profile. Secondly, the graphene nanoflakes were characterized by Raman spectroscopy to comprehend the substance type. Finally, The graphene nanoflakes were characterized by SEM to comprehend the distance between the Au electrode.

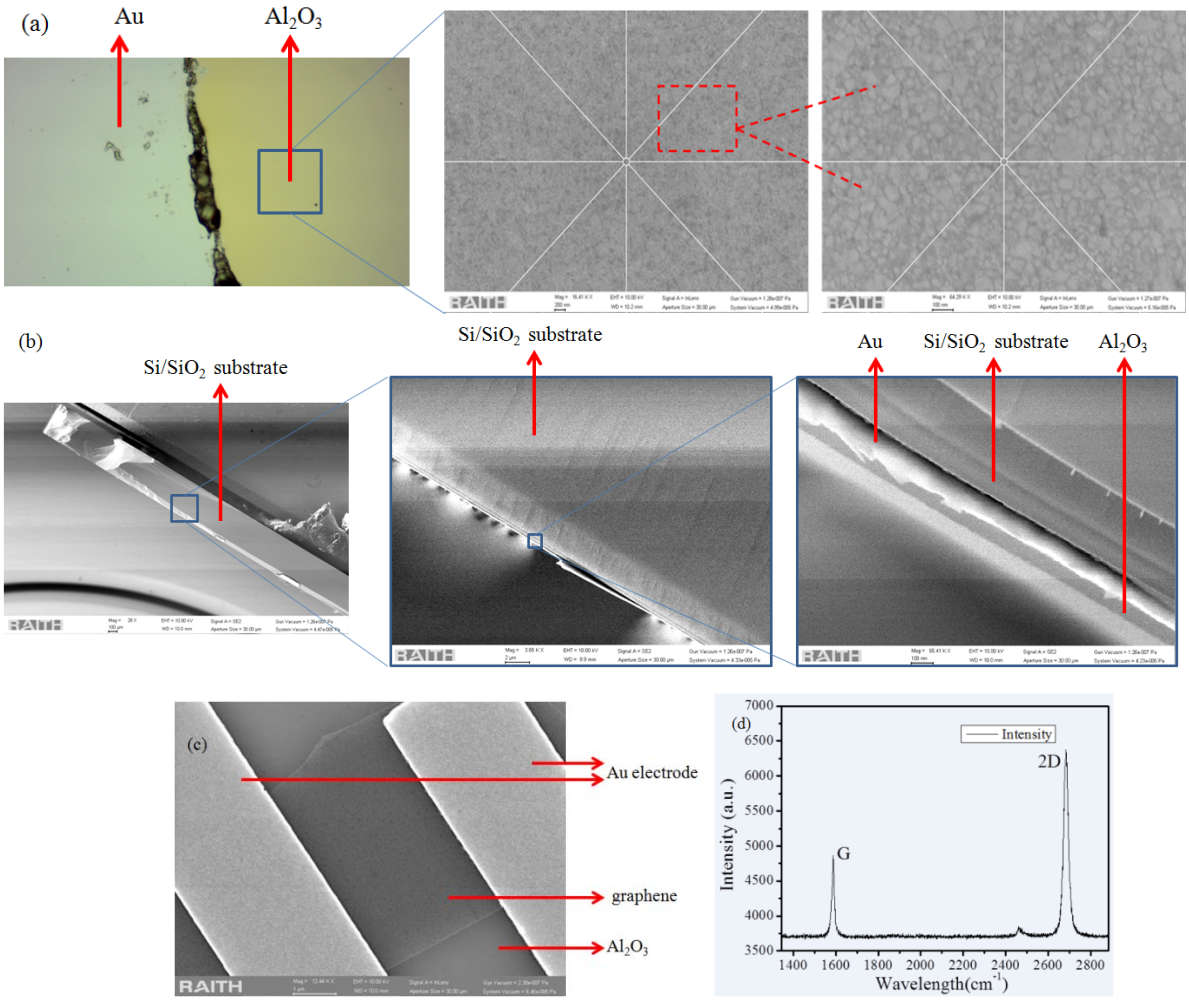

Figure 2. Characterization of monolayer graphene nanoflakes and FETs. (a) Photography of the interface of Al_2O_3-Au in the top view under optical microscope and its SEM image in 16.41k X and 64.29k X magnification. (b) SEM image of the interface of Al_2O_3-Au-Si/SiO_2 in the side view in 28 X, 3.65k X and 65.41k X magnification. (c) SEM image of the back gate of DG-FET in the top view (h) Raman spectra of monolayer graphene.

Results of characterization: Firstly, figure 2(a) shows the photography of the interface of Al_2O_3-Au in the top view under optical microscope and its SEM image in 16.41k X and 64.29k X magnification and there is a clear boundary between the two regions. And the Al_2O_3 film is smooth and compact. Secondly, figure 2(b) show the SEM image of the interface of Al_2O_3-Au-Si/SiO_2 in the side view in 28 X, 3.65k X Thirdly, figure 2(c) shows the SEM image of the back gate of DG-FET and the production of the back gate of DG-FET is successful. Finally, figure 2(d) shows the raman spectra of monolayer graphene and proved that it is indeed graphene.

Summary

To summary, we have fabricated DG-FETs based on monolayer graphene. Due to the unique structural properties of two-dimensional material, DG-FETs based on it exhibit a high gate modulation (On/Off ratio is large), and higher regulation accuracy. In our experiment, we fabricated DG-FETs by standard micro-nano technology and characterized it by SEM and Raman spectra. Obviously, we fabricated DG-FETs with great quality based on monolayer graphene successfully. And our next task is to study its electrical properties in depth. In all, the new preparation method to

product double-gate field effect transistor, we believe, will open up a new way in the application of FETs.

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