

Design of Video Acquisition System Based on ARM

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Abstract. At present, the video acquisition and compression system which is based on PC achieve the purpose of video capture through a dedicated video capture card by using PC's powerful data processing capabilities and its marvelous interface. Although the PC-based system is currently widely used and with a strong processing power, it can't meet the requirements in many occasions because its great power consumption, high cost and the need for personal maintenance and management is incompatible with present developing trend as instrument miniaturization, low power consumption and portability. Based on the combination of the development and practical application of video image technology and the requirement of the system and the specific comparison of the advantages and disadvantages of various schemes, this paper proposes a design scheme of embedded video acquisition system based on ARM.

Introduction

In recent years, with the rapid development of communication technology, microelectronics technology and computer technology, the network bandwidth and storage capacity have been greatly improved, and with the increasing cross linkage among electronic, communication and broadcasting, the world entered an All-Digital network era. At the same time, digital multimedia technology has also been rapidly developed and gradually penetrated into the life, work and learning of human beings in all aspects, and it is changing people's traditional way of life. People's need for video conferencing, video telephony, digital TV broadcasting and other multimedia technology becomes more and more widely. However, the information and data volume is huge in the field of multimedia technology especially in the field of digital video, and requirement about the processing capacity and storage capacity is extremely high, so if an effective code compression not be processed, communication and transmission would encounter great difficulties, and thus it can't meet the needs of people.

In the basis of the detailed analysis of the development status of video capture system in China and abroad, and the fact that PC platform system is difficult to meet the increasingly complex and extensive image processing applications, this essay proposes a design scheme of embedded platform video acquisition system based on ARM. By taking full advantage of the embedded platform integration, low power consumption, multi-tasking operating system supported and the most advanced JPEG2000 encoding compression algorithm, the scheme is trying to fulfill a small, low-cost, integrated video image acquisition and compression system through designing some appropriate hardware and software to meet our needs for video capture and compression. The research of this system has an important reference value and guiding significance for boosting the instrumentation of video capture system and promoting the development of related industry.

Video Acquisition

Signal captured by the analog video camera is an analog one, which includes not only the image signal but also the synchronization signal, the line blanking signal, the field synchronization signal and the field blanking signal. Consequently, Video input processing in video capture is very important. The traditional video input processing module uses discrete components and so the circuit is very complex and poor reliable and is not easy to debug. Today, many well-known semiconductor manufacturers integrate these complex video A / D conversion circuit into one chip to produce the video capture chip, which provides great convenience to subsequent image

processing. Video capture chips in market at now has ones like SAA711X system products from PHILIPS, EM2820 from EMPIA of Taiwan and TW6802 from TECHWELL of the USA and so on. Though research, products from PHILIPS was found to be the best in respect of product performance and cost effectiveness, and so the video capture chip SAA7113H from PHILIPS is chosen to design the video capture part.

As a representative one in PHILIPS' video decoder chip series, SAA7113H is being used in many video products as TV cards, MPEG2, MPEG4, and the chip forms an application system with the usage of CMOS technology and through the connection of I2C bus and PC or control chip with I2C bus interface. With two analog processing channels inside, the chip is able to bring out following applications: Video source selection, Anti-aliasing filtering, Analog-to-digital conversion (A / D), Automatic clamping, Automatic gain control (AGC), Clock generation (CGC), Multi-format decoding, Brightness / Contrast / Saturation Control (BCS), and Multi - standard VBI data decoding. The main role of SAA7113H is to decode the entered analog video signal into a standard "VPO" digital one, and this makes the chip an equivalent of an "A/D" device. Because of its compatibility with various video standards worldwide, the chip's internal registers needs to be configured in accordance with Chinese video standards if be used in China or it can't be output as required. Programmable acquisition chip SAA7113H mainly has the following characteristics:

1. It has four analog input channels, and is able to select internal analog signal source, such as: $4 \times$ CVBS, $2 \times$ Y / C or ($1 \times$ Y / C and $2 \times$ CVBS). With the configuration of I2C bus on register sub-address 02H, we can get the on-chip signal source that is demanded. CVBS (automatic gain) way, as shown in Fig. 1 :

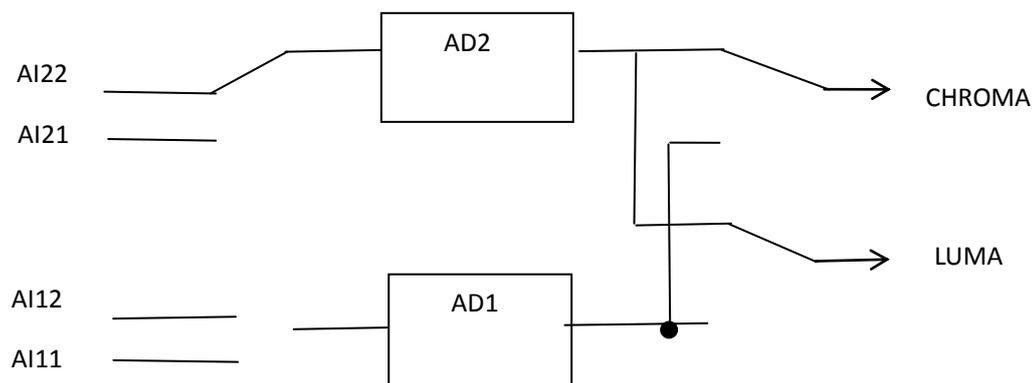


Figure 1. Video Input Connecting Way

2. It can make a Static gain control or automatic gain control on he selected CVBS (or Y / C) channels through programming, and there are two built-in analog anti-aliasing filters in it.

3. Two 9-bit CMOS analog-to-digital converter, digital CVBS or Y / C signal is output to the VPO port through the I2C bus control.

4. SAA7113H can output a variety of data formats, through the control of the I2C bus control, you can output from the VPO bus standard ITU-R BT 656YUV4: 2: 2 format digital video.

5. The two multi-function real-time output ports RST0, RST1 controlled by the I2C can output put where the port field signal and synchronization signal and so on.

6. Only one 24.576MHz crystal oscillator is needed for different format standards.

7. The rate of the I2C bus which is read and written by the external controller is up to 400kbps.

Hardware Structure of the System

According to the general method for video system functional structure division, the video acquisition system hardware can be divided into the following modules: 1. acquisition module, 2. control module, 3. transmission module, 4. other modules. Video decoder chip SAA7113H is used in the video acquisition module which converts the analog signal captured from external CCD into

digital signals under the control of video capture master controller S3C44B0X and ADV202. The chip S3C44B0X is used to make communication with ADV202 and at the same time to control the work of SAA7113H. The image data is sent to the host computer by connecting USB interface to the host computer. Here is the system diagram displayed in Fig. 2 :

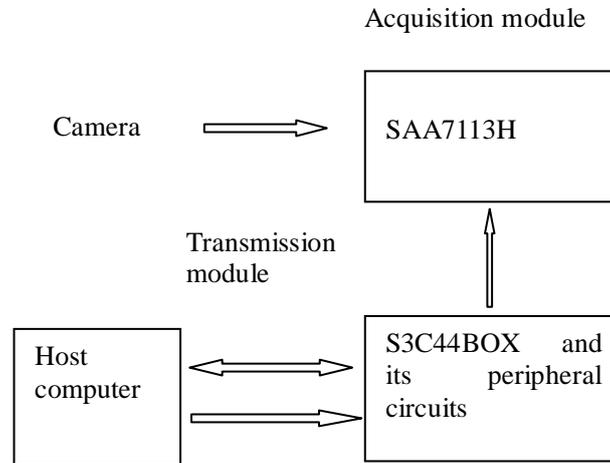


Figure 2. system diagram displayed

Designation of the Video Acquisition Module

Considering Factors in the Designation of the Video Acquisition Module. The first fact of the designation is A/D transformation of signals thanks to the use of integrated processing chip SAA7113H that makes the video signal's A/D transformation be very convenient through setting the chip internal register.

When it is powered on, the chip SAA7113H is not immediately capturing the analog video signal for A / D conversion processing or digital signal output but can work properly only after the initialization of the internal storage department taken by the I²C serial bus.

A. I²C serial bus

Because the I²C bus interface is provided by the main controller S3C44B0X, SAA7113H can be connected directly to the corresponding pin of the S3C44B0X via the SCL and SDA signal lines. It is as shown in Fig. 3 below:

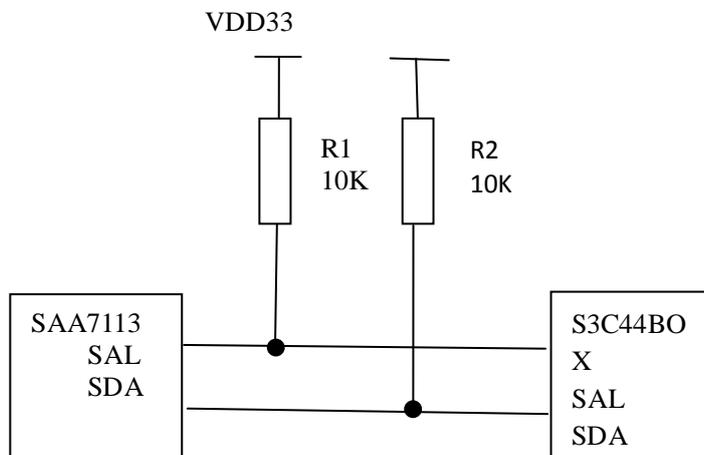


Figure 3. The I²C interface connection diagram

B. Output data format

With 8-bit VPO bus width, SAA7113H has an output format of standard ITU-R BT 656 YUV4:

2: 2 video data. The chip SAA7113H has 720 pixels per active scan line and outputs a Byte decoded data on the rising edge of each LLC. Each of the pixels needs 2 LLC cycles and has its own luminance data Y, but each two adjacent pixels in output data share the same color difference data CB, CR. So it can be thought that the data of each pixel can be expressed by two consecutive Byte, but if when the format needs a transmit to RGB or other processes, it is the set of color difference data CB_{2n} , CR_{2n} ($n = 0, 1, 2, \dots$) shared by the pixels number $2n$ and $2n+1$ correspondingly makes correct processes. The structural format is shown as below Table 1:

Table 1 the Output Data Format of SAA7113H

720 Pixels YUV 4:2:2 data								
C_{B0}	Y0	C_{R0}	Y1	C_{B2}	Y2	C_{R718}	Y719

Conclusion

Embedded device has advantages like small size, low cost, stable performance, hardware and software replaceable, etc., and has a broad market of application and development prospects. However, its application areas is too constrained because that network video image acquisition technology based on personal computer is restricted by PC's low software stability and non-targeted hardware resources which causes wastes. In the contrary, the advantages of the embedded technology can just to make up for the shortcomings brought by personal computers, so in order to make further development and expand application areas, combining video image acquisition system and embedded technology and using all kinds of good points of embedded technology becomes an important direction of development for network video image acquisition system in the future.

References

- [1] Sangiovan nivin centel li A, Natale M D. Embedded System Design for Automotive Applications[J]. Computer, 2007, 40(10):42-51.
- [2] Malinowski A, Yu H. Comparison of Embedded System Design for Industrial Applications[J]. IEEE Transactions on Industrial Informatics, 2011, 7(2):244-254.
- [3] Marwedel P. Embedded Systems Foundations of Cyber-Physical Systems[J]. Embedded System Design, 2010, 3(2):260.
- [4] Ingham M D, Rasmussen R D, Bennett M B, et al. Engineering Complex Embedded Systems with State Analysis and the Mission Data System[J]. Journal of Aerospace Computing Information & Communication, 2015, 2(12):507--536.
- [5] Pimentel A D, Erbas C, Polstra S. A. Systematic Approach to Exploring Embedded System Architectures at Multiple Abstraction Levels[J]. IEEE Transactions on Computers, 2006, 55(2):99-112.
- [6] Kocher P, Lee R, Mcgraw G, et al. Security as a New Dimension in Embedded System Design[C]. Design Automation Conference. ACM, 2004:753-760.
- [7] Henkal J, Wolf W and Lekatsas H. Code Compression for Low Power Embedded System Design[C]. Design Automation Conference, 2000. Proceedings. IEEE, 2000:294-299.

- [8] C.E Lin, C.C Li and Wu C C, et al. A real time GPRS surveillance system using the embedded system[C]. Industrial Electronics Society, 2003. IECON '03. the, Conference of the IEEE. IEEE Xplore, 2012:1228-1234 Vol.2.
- [9] Hines K, Borriello G. Dynamic Communication Models in Embedded System C
- [10]Narayanan V, Y Xie, Reliability concerns in Embedded System Designs[J]. Computer, 2006, 39(1):118-120.
- [11]Vidal, Jorgiano, Lamotte D, et al. A Co-design Approach for Embedded System Modeling and Code Generation with UML and MARTE[J]. 2009:226-231.
- [12]Sung W T, Hsu Y C. Designing an Industrial Real-time Measurement and Monitoring System Based on Embedded System and ZigBee[J]. Expert Systems with Applications, 2011, 38(4):4522-4529.