An SEU Hardened 65nm/4T-SRAM Cell for High Reliable Space Applications

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Abstract. A novel mono-stable 4T-SRAM cell is proposed in this paper. The cell is designed in 65nm LPCMOS process and simulated to find out the linear energy transfer threshold of SEU. T-CAD simulation results show that its LET_{th} for data(1) is up to 41.6 MeV/mg/cm^2 , almost the same as DICE, and the data error rate can be reduce to $1.2 \times 10^{-11}/\text{bit.day}$ with a particular duplication redundancy SRAM structure. The proposed 4T cell takes advantage of small cell size and solid anit-SEU ability, showing good potential to be used in SEU hardened SRAM.

INTRODUCTION

SRAM is widely used in the space electronics systems. As the feature size of SRAM process scaled down, linear energy transfer threshold (LET_{th}) of single-event-upset (SEU) decreases rapidly, due to the bi-stable structure in traditional 6T-SRAM cell [1]. Studies show that when process shrinks from $0.8\mu\text{m}$ to 65nm, LET_{th} drops from 57.1 to less than 1.73 MeV/mg/cm^2 [2, 3]. In order to improve anti-SEU ability of SRAM cell, Quatro (10T) structures and 11T structures [4] are proposed, but their LET_{th} is still smaller than 10 MeV/mg/cm^2 , resulting in high SEU error rate caused by high flux particles in the space environment, such as C1 ($LET=12.6 \text{ MeV/mg/cm}^2$). Besides, Dual Interlocked storage Cell (DICE) and DICE with guard ring [5] are developed to increase LET_{th} up to 40 MeV/mg/cm^2 , while their cell size is as larger as 10X of 6T-SRAM cell, limiting its application for large capacity SRAM.

In this paper, we firstly propose a novel mono-stable four-transistor (4T) SRAM cell, which has advantages in small cell size and solid anit-SEU ability. The cell is designed in 65nm LPCMOS process and simulated with Technology Computer Aided Design (T-CAD) simulation tools. Simulation results exhibit significant improvement in LET_{th} of SEU, therefore show good potential to be used in SEU hardened SRAM.

4T-SRAM CELL DESIGN

The 4T-SRAM cell is designed based on 65nm LPCMOS process, wherein data are stored in Q and Q_N , as shown in Figs. 1(a) and (c). Compared with traditional 6T-SRAM cell, two feedback transistors are removed to make it work in a mono-stable mode; i.e. data(1) ($Q=1$; $Q_N=0$) is held stably with the feedback of N1 and P1, while data(0) ($Q=0$; $Q_N=1$) is unstable due to Q and Q_N being float. In order to store '0' stably, device parameters and operation conditions, such as V_{th} , W/L, V_{DDI}/V_{SSI} and V_{WWL}/V_{RWL} , are optimized to ensure that I_{leak} of NG1/PG1 are larger than the one of P1/N1 in any situation. Thus, I_{leak} of NG1 and PG1 help to maintain '0' stably.

The write and read operation scheme is dedicatedly designed to prevent data(0) loss in the unselected cells. Both write and read operations are performed in a single-end mode; wherein the write data(1/0) on WBL is written in the selected cell through NG1 with $WWL=1$, while the read data is output to RBL through PG1 with $RWL=0$. To realize single-end-mode read, reference cell (RefCell) is introduced into the array with V_{Ref} being about 0.6V, as shown in Fig. 1 (b). Fig.2 shows the detailed write/hold/read operation waveforms, which illustrates the good function of the cell.

Considering the space radiation, 4T-SRAM cell also features with asymmetric single-event-

effect of data 1/0; i.e. data(1) is tolerant while data(0) is sensitive to SEU. For data(1), assuming the drain of NG1 is hit by a high energy particle, Q flips to '0', while Q_N keeps in '0' without the feedback from Q; then Q will recover to '1' through the feedback of P1. For data '0', assuming the drain of P1 is hit, Q flips to '1', and Q_N flips to '0' subsequently due to the feedback of N1, resulting in an SEU finally, as illustrated in Fig. 3. According to the discussion above, it's no doubt that the SEU error rate has the relationship: $r(0) \gg r(1)$, where $r(1)$ and $r(0)$ describe the SEU rate of data (1) and data (0), respectively.

Based on the asymmetric SEU features of the 4T-SRAM cell, duplication redundancy SRAM system can be structured to increase the anti-SEU ability, as presented in Fig. 4. Data is stored in two duplicated blocks, read data of each are sent to an AND gate to derive final data. As far as data(0) in the two blocks don't upset simultaneously, it can be read out correctly. For the duplication redundancy hardened system, the final data error rate $p(1)$ and $p(0)$ can be calculated as: $p(1) = 1 - [1 - r(1)]^2 \approx 2r(1)$ and $p(0) = r^2(0)$.

FIGURE 1. Schematic of (a) Cell and (b) RefCell **FIGURE 2.** Simulation of write, hold and read. (c) Cell layout.

	Store '1'		Store '0'	
	Q	QN	Q	QN
Original Data	'1'	'0'	'0'	'1'
Particle Hits				
Drain(NG)			Drain(P1)	
No FB			FB(N1)	
	'0'	'0'	'1'	'0'
			FB(P1)	
Final Data	(recover) '1'	FB(P1) '0'	'1'	'0'

FIGURE 3. SEU characteristics of data 1/0.

FIGURE 4. Duplication redundancy SRAM for SEU hardened.

SIMULATION RESULTS

As the process scaled down, the charge sharing effects and the parasitic BJT effects intensify and increase the SEU cross-section of the SRAM cell [6]. The SEU cross-section and data error rate are traditionally evaluated with T-CAD simulation methods. In this paper, T-CAD simulation is also used to find out the exact LET_{th} of the proposed 4T cell, with a well-known T-CAD tool developed by Cogenda Co. [7].

Based on the cell layout as shown in Fig. 1(c), a 3D macro model of a 5×5 mini array is firstly built, as Fig.5 presents. The target cell for simulation is surrounded by two columns and two rows of dummy cell that contains only pick-ups. Parameters of the transistors are derived from the real data of the 65nm process, and calibrated by comparing simulated I-V curves with measured data. During simulation, data 1/0 is written into the cell beforehand, then the cell stays in hold state, and particles of different LET are injected to the whole cell region. Geant4 [8] does Monte Carlo simulations of the transmission of high-energy particles, and a fast solver [9], which solves the full

T-CAD equations, accomplishes fully physical simulation.

FIGURE 5. 3D model of the proposed 4T-SRAM cell.

Fig. 6 (a), (b), (c) and (d) are the simulation results, wherein circles and squares are the points where the particle hits, and the darker they are, the data is more likely to flip; squares means data upset finally, while the dark circles means flips midway and recovery in the end. LET_{th} of '0' is 0.41 MeV/mg/cm^2 , approximating the value of 65nm 6T-SRAM cell [3]; while LET_{th} of '1' is 41.6 MeV/mg/cm^2 , approximating the value of 65nm DICE cell [5]. Studies show that the parasitic BJT effect triggered by large energy particles is the real mechanism to cause the data(1) upset [10]. Compared with 65nm cells of 6T [3], Quatro [4] and DICE [5], LET_{th} of data(1) is almost the same as DICE, while dual-4T cell size is only 12.5% to DICE, as Table 1 shows.

FIGURE 6. (a) Hold '0', particle α , $LET=0.32 \text{ MeV/mg/cm}^2$, no flip. (b) Hold '0', particle α , $LET=0.41 \text{ MeV/mg/cm}^2$, 3 flips. (c) Hold '1', particle Cu, $LET=31.9 \text{ MeV/mg/cm}^2$, no flip. (d) Hold '1', particle Br, $LET=41.6 \text{ MeV/mg/cm}^2$, 4 flips.

Based on the simulated LET_{th} , the SEU cross section and the data error rate can be calculated, as shown in Fig. 7. In geosynchronous orbit, '1' SEU rate is approximately $1.8 \times 10^{-13}/\text{bit.day}$, while '0' SEU rate is $3.5 \times 10^{-6}/\text{bit.day}$. With duplication redundancy hardening, data(0) error rate can be reduce to $1.2 \times 10^{-11}/\text{bit.day}$, lower than the space application requirement of $10^{-10}/\text{bit.day}$.

TABLE 1. LET_{th} and cell size comparison of 4T, 6T, Quatro and DICE.

Structure	Normalize d Cell Size (/6T)	LET_{th} (MeV/mg/cm^2)	
		'0'	'1'
4T (This Work)	2×0.72	0.41	41.6
6T [3]	1	< 1.73	< 1.73
Quatro [4]	1.5	< 4	< 4
DICE [5]	11.5	40(test)	40(test)

FIGURE 7. Cross section of 4T cell with particle hitting vertically.

CONCLUSION

A 65nm mono-stable 4T-SRAM cell is studied, which takes advantage of small cell size and

solid anit-SEU ability. T-CAD simulation results show that its LET_{th} for data(1) is up to 41.6 MeV/mg/cm², almost the same as DICE, and the data error rate can be reduce to 1.2×10^{-11} /bit.day with a particular duplication redundancy SRAM structure, showing good potential to be used in SEU hardened SRAM.

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REFERENCES

- [1] Li T., et. Al., A CMOS triple inter-locked latch for SEU insensitivity design. *IEEE TNS*, 2014, 61(6):3265-3273.
- [2] Zheng Z., et. Al., Comparison of decoupling resistors and capacitors for increasing the single event upset resistance of SRAM cells. *2015 IEEE 11th Int. Conf. on ASIC (ASICON)*, 2015:1-3.
- [3] Gnima T., et. Al., Simulation of Single and Multi-Node Collection: Impact on SEU Occurrence in Nanometric SRAM Cells. *IEEE TNS*, 2011, 58(3):862-869.
- [4] Li L., et. Al., A Novel Asymmetrical SRAM Cell Tolerant to Soft Errors. *IEEE 28th Canadian Conf. on Electrical and Computer Engineering (CCECE)*, 2015:1403-1408.
- [5] Maxim S. G., Anna B. B., Pavel S. D., Semi-Empirical Method for Estimation of Single-Event Upset Cross-Section for SRAM DICE Cells. *IEEE TNS*, 2016, 63(4): 2250-2256.
- [6] Lin L., et. Al., Highly-Scaled SRAM immunity to MNU based on analysis of an induced parasitic bipolar effect. *2nd Int. Conf. on Communication Systems, Networks and Applications (ICCSNA)*, 2010:316-320.
- [7] Information on <https://www.cogenda.com/>
- [8] Allison J., et. Al., Geant4 developments and applications. *IEEE TNS*, 2006, 53(1):270-278.
- [9] Ding G., Chen S., Full-TCAD Device Simulation of CMOS Circuits with a Novel Half-Implicit Solver. *The Int. Conf. on Simulation of Semicon. Processes and Devices (SISPAD)*, 2012:272-275.
- [10] Hong X., et. Al., Simulation and research on a 4T-cell based duplication redundancy SRAM for SEU radiation hardening. *Journal of Semiconductor*, 2015, 36(11):114003-114005.