A Low Power and High Accuracy Threshold Voltage Detection Circuit for Flash Memory

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Abstract. A low power threshold voltage detection circuit and its accuracy optimization method for NOR flash memory are proposed in this paper. The whole circuit system is composed of data path, ramp voltage generator, and other auxiliary circuits. This memory system with 256Mb cells is simulated in a 65nm 2P3M NOR flash memory process. The simulation results show that the proposed circuit and optimization method achieve low power consumption with a relatively high accuracy.

I. INTRODUCTION

Although taken into applications for many years, flash memory continuously confronted increasing problems and challenges [1, 2]. For example, the progress in chip manufacturing processes results in considerable capacitance and crosstalk between neighbor cells. Besides, in order to attain higher storage density and lower cost, MLC (multiple level cell) and TLC (triple level cell) emerge, which means that data detention, endurance and failure mode should be paid more attention to. These problems can be reflected in threshold voltage distribution of cells [3]. As a result, threshold voltage measuring method and circuit is vital. However, traditional threshold voltage measuring methods for flash memory always have shortages, such as high power, low accuracy, and large area [4].

This paper proposes a low power and high accuracy threshold voltage detection circuit and its accuracy optimization method. Section II puts forward a detailed introduction of this new threshold voltage detection circuit and its operation principle. Then in Section III, two methods for accuracy optimization are demonstrated to make correction of output data and promote readout resolution. Finally, conclusion is made in Section IV.

II. THRESHOLD VOLTAGE DETECTION CIRCUIT

The data path of proposed threshold voltage detection circuit and its timing diagram are shown in Figure 1. After WL and BL decoder get the command of timing logic controller to select a page of memory cells, signal Prech instantaneously goes high, which controls transistor M_2 to precharge readout capacitor C_{Read} to V_{DD}, and BL voltage V_{BL} to a voltage about 0.2V (equal to reference voltage $V_{refClamp}$ subtracts threshold voltage V_{thm1} of transistor M_1). After Prech goes low, the counter will begin to work, and V_{ramp}, generated from ramp voltage generator, will begin to rise. After V_{ramp} reaches the threshold voltage of a selected memory cell, the readout capacitor C_{Read} will discharge through this memory cell, and the voltage V_{N2} on node N2 will decrease. When V_{N2} is lower than reference voltage $V_{refComp}$, the output of the comparator will go low, which stops the counter. As a result, the threshold voltage of the selected memory cell is converted to the count number D_{out} of the counter and then will be stored in the register. In the proposed design, the counter is 9-bit, and the ramp voltage V_{ramp} ranges from low bound Vstart to up bound Vend. The threshold voltage of the selected memory cell is digitalized as Equation (1):

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$$D_{out} = \frac{V_{th} - V_{start}}{V_{end} - V_{start}} \times 2^9 \tag{1}$$

where V_{th} is the threshold voltage of the selected memory cell. The proposed circuit achieves low power because the power consumption mainly comes from precharging readout capacitor C_{Read} to V_{DD} and BL parasitic capacitor C_{Par} to 0.2V. The structures of the comparator and counter are simple, which consume very little power.

To generate appropriate and various ramp voltages for the data path, an adjustable ramp voltage generator is proposed as shown in Figure 2. It is composed of operational amplifier, capacitance and adjustable resistances. When signal Prech is high, the ramp voltage V_{ramp} equals to a reference voltage of V_{refWL1}. When signal Prech goes low, V_{ramp} begins to rise. This procedure follows Equation (2):

$$V_{ramp} = V_{refWL1} + \frac{V_{refWL1} - V_{refWL2}}{RC} t \tag{2}$$

By changing reference voltage V_{refWL1}, V_{refWL2} and resistances, we can get ramp voltages with different slope to read out the cell's threshold voltage.

The proposed circuit works at a frequency of 100MHz. Simulation results show that the average current of the proposed data path is 3.12μA, which is extremely low in comparison to traditional methods.

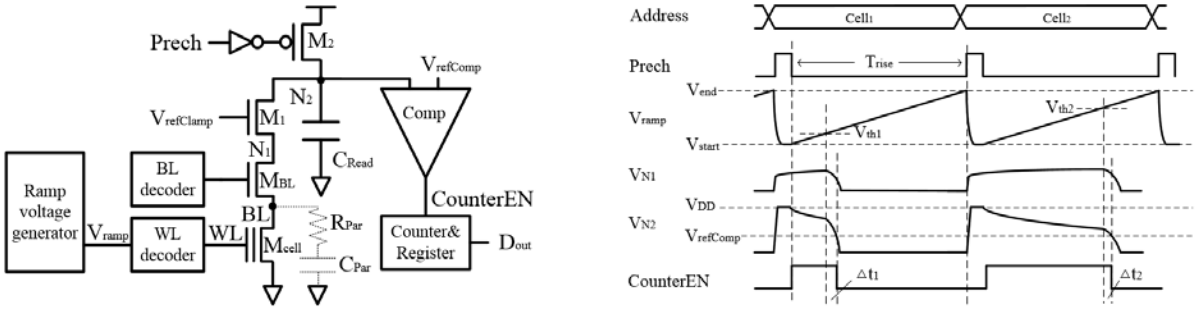

FIGURE 1. (a) Schematic of the data path. (b) Timing diagram.

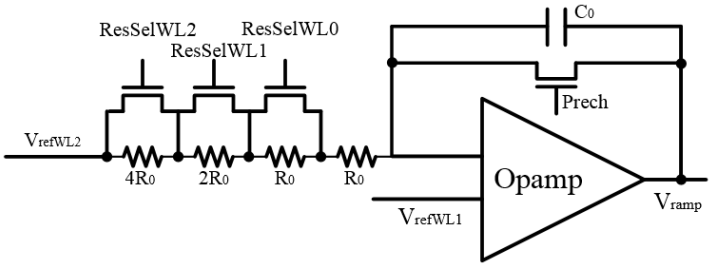

FIGURE 2. Schematic of ramp voltage generator.

III. ACCURACY OPTIMIZATION METHOD

In this section, two methods to optimize accuracy for this threshold voltage detection circuit will be presented. The first method called accuracy calibration method will be explained here. When ramp voltage V_{ramp} reaches the threshold voltage of the selected memory cell, V_{N2} will not decline from V_{DD} to $V_{refComp}$ immediately, because of the limited current of the memory cell and transistor M_1. As a result, a deviation exists between the threshold voltage of the memory cell and the count number. In Figure 1, M_1 is used to clamp V_{N1} to a voltage about 0.2V (equal to reference voltage $V_{refClamp}$ subtracts threshold voltage V_{thm1} of transistor M_1), instead of using an amplifier [5]. Thus, V_{N1} and V_{BL} cannot be precharged to the stable voltage 0.2V within a limited precharge time. As a result, in the time interval between signal Prech going low and V_{ramp} reaching the threshold voltage of selected memory cell, there is a small current flowing from C_{Read} to C_{Par} through M_1, which raises V_{N1} closer to 0.2V and makes V_{N2} decline. When V_{ramp} goes higher than the threshold voltage of selected memory cell, C_{Read} and C_{Par} begin to discharge to ground through the selected memory cell. Then V_{N2} declines lower than reference voltage $V_{refComp}$, and the output of the

comparator goes low, which stops the counter. As a result, the threshold voltage of the selected memory cell is smaller than the count number of the counter. Figure 3(a) shows the waveform of V_{N2} after signal Prech goes low for two memory cells with different threshold voltages. It demonstrates that $cell_1$ with smaller threshold voltage exhibits a worse deviation than $cell_2$ with bigger threshold voltage. Figure 3(b) shows the relationship between the threshold voltage and the count number D_{out}.

The second method called multi-range method can improve detection resolution further on. We define the threshold voltage detection resolution as:

$$R_{th} = \frac{\Delta D_{out}}{\Delta V_{th}} = \frac{2^9}{V_{end} - V_{start}} \tag{3}$$

If we want to get a higher detection resolution, we need to decrease the range of V_{end}-V_{start}.

Let us suppose that a 256Mb memory cells has an initial threshold voltage range from V_{th1} to V_{th2}. If we set the ramp voltage V_{ramp} from V_{start} to V_{end} as line L_1 shown in Figure 4(a), we can get the threshold voltage distribution of the memory array as line L_3, and the detection resolution is $2^9/(V_{end}$-$V_{start})$. If we set the ramp voltage V_{ramp} from V_{th1} to V_{th2} as line L_2, we can get the threshold voltage distribution of the memory array as line L_4, and the detection resolution is improved to $2^9/(V_{th2}$-$V_{th1})$. Figure 4(b) shows the simulation result of the threshold voltage distribution of the 256Mb memory cells in two ramp voltage ranges.

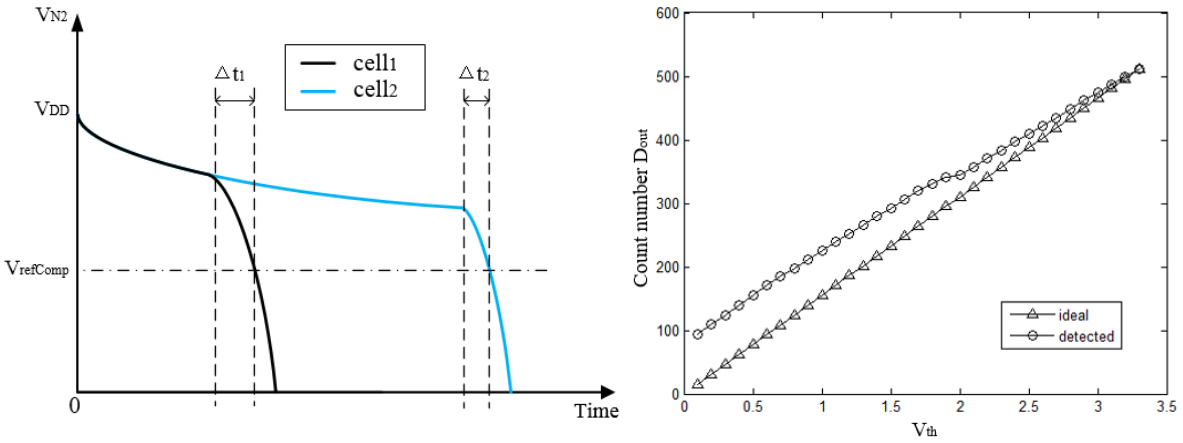

FIGURE 3. (a) Deviation comparison of reading two cells. (b) Ideal and detected count number D_{out}.

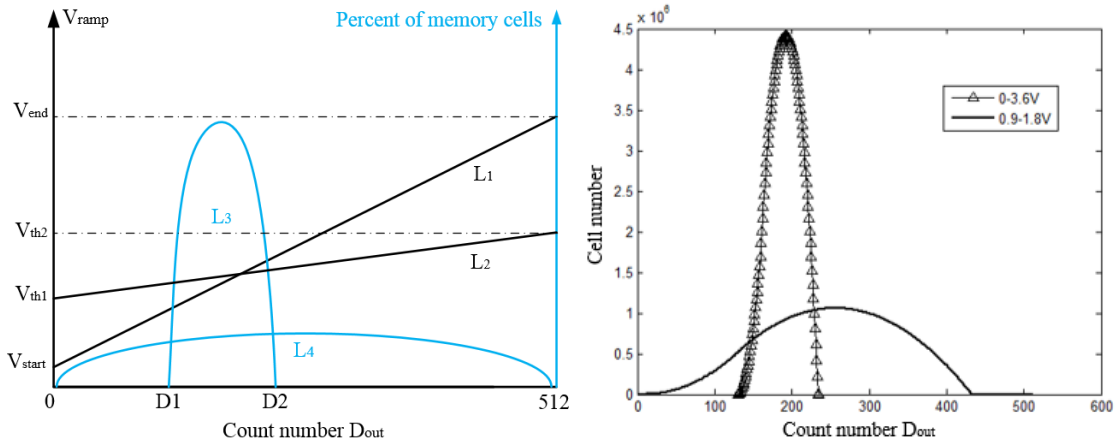

FIGURE 4. (a) V_{th} distribution with different V_{ramp} ranges. (b) Simulation result of V_{th} distribution.

IV. CONCLUSION

In this paper, a low power threshold voltage detection circuit and two accuracy optimization

methods for a 256Mb NOR flash memory are proposed. Simulation results show that this detection method can achieve the goal of threshold voltage detection with high resolution. Since distribution information of the threshold voltage is important for planning threshold voltage of memory cells in program/erase state, and studying endurance and retention characteristics of the memory cells, the proposed circuit and method are helpful for researches to achieve these goals.

V. ACKNOWLEDGEMENTS

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