

Research on tracking of spread spectrum PN code signal

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Abstract. In this paper, the advanced-lagged incoherent DDLL is discussed. By analyzing and simulating the phase characteristics and steady-state characteristics, we can determine the parameters such as tracking interval, loop bandwidth and so on to ensure that the code ring accurately tracks the input signal code Phase change.

Introduction

Tracking PN code phase is often based on delay-locked loop to achieve, the principle is to generate phase lag in the local and phase ahead of the two signals, the receiver input signal and the two signals do correlation operation, comparing the two results, resulting in PN Code of the phase error, the final control of the local NCO generated by the local signal and the input signal phase of the symbol to maintain consistency.

Structure of delay-locked loop

DLL tracking principle: PN code using the autocorrelation properties, phase detector PN code can get the phase error, the error is filtered to control the local NCO, and the final phase error is eliminated. The general structure is shown in Figure 1. For ease of analysis, it is assumed that the signal after the carrier is stripped has only the PN code and noise, and the tracking is performed without considering the influence of the information data.

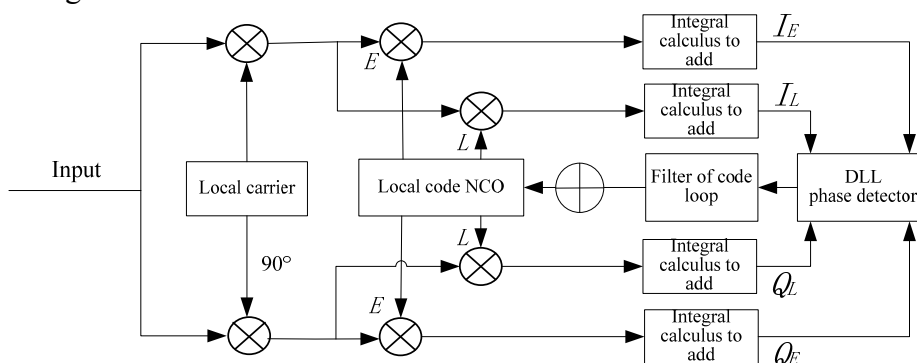


Figure 1. Block diagram of the PN code tracking loop

Figure 1 phase detector function is based on the PN code auto-correlation properties to achieve, the specific characteristics of the demonstration shown in Figure 2. The phase characteristics of the autocorrelation function of the spread spectrum sequence which deviates by half a symbol are shown by the dotted line (1) in the figure; 2). The two shifted autocorrelation functions are summed to obtain the phase trace of the spread code phase trace, which is represented by a solid line in the figure.

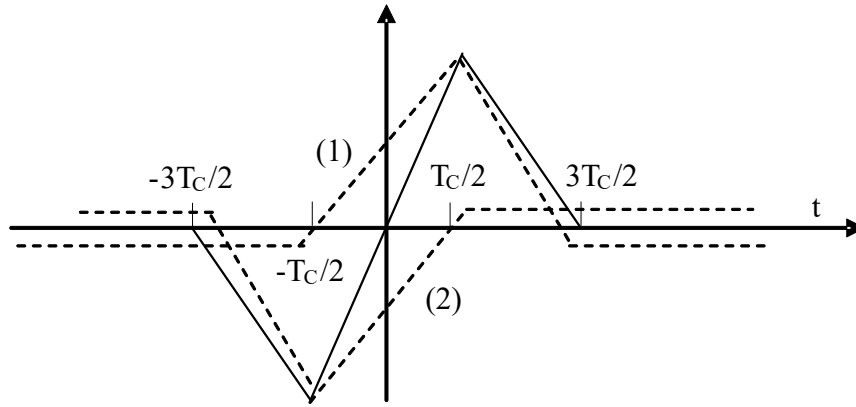


Figure 2. S-curve of the phase detector

Analysis of PN code phase detector

Table 1 summarizes the three types of delay-locked loop phase discriminator and their characteristics.

Table 1. General Delay-Locked Loop Detector

Phase detector algorithm	characteristic
$\sum (I_{ES} - I_{LS})I_{PS} + \sum (Q_{ES} - Q_{LS})Q_{PS}$	Point product power phase detector. The DLL phase detector with three correlators, which greatly reduces the amount of computation. When the correlator spacing is equal to 0.5 base code, this time has the closest error output.
$\sum (I_{ES}^2 + Q_{ES}^2) - \sum (I_{LS}^2 + Q_{LS}^2)$	Advanced phase - delay power detector. And the tracking performance is sensitive to the amplitude of the signal in the range of ± 0.5 base code, but the tracking characteristic of the phase detector is sensitive to the signal amplitude.
$\sum \sqrt{I_{ES}^2 + Q_{ES}^2} - \sum \sqrt{I_{LS}^2 + Q_{LS}^2}$	The envelope detector is advanced by subtracting the hysteresis. It has a large amount of computation. When the correlator spacing is equal to 0.5 base code, it has better tracking error.

Error analysis of dynamic introduction

The error of the tracking loop introduced by the dynamic code is related to the loop bandwidth and the order of the loop. The tracking error introduced dynamically can be expressed as:

$$R_{em} = \frac{d^m R / dt^m}{\omega_N^m} \quad (\text{deg}) \quad (1)$$

In the formula, the unit of the molecule is $\text{chips} / \text{s}^m$, m is the loop order, the denominator is the loop natural angular frequency.

Formula: $3\sigma_{DLL} = 3\sigma_{iDLL} + R_e \leq d / 2 (\sigma_{DLL}$ is the root mean squared error of the measurement, σ_{iDLL} is the root mean square of the noise introduction error, R_{em} is the error introduced by the receiver in the code tracking loop). The dynamic performance threshold can be derived:

$$R_{em} \leq d / 2 - 3\sigma_{iDLL} \quad (2)$$

That is:

$$d^m R / dt^m \leq \left[\frac{d}{2} - 3 \sqrt{\frac{B_n d}{2c / n_0} \left[1 + \frac{2}{(2-d)c / n_0 T} \right]} \right] \times \omega_N^m$$

Since the distance of a pseudocode chip is:

$$\lambda = \frac{c}{R_{PN}} = \frac{3 \times 10^8}{5.115 \times 10^6} = 586.5(m) \quad g = 9.8m / s^2$$

The dynamic tolerance of the third-order tracking loop with different signal-to-noise ratio, bandwidth and correlation interval can be obtained.

The dynamic tolerance of third-order tracking loops with different code correlation intervals and different carrier-to-noise ratios are simulated respectively. The code correlation interval is $\frac{d}{2} T_c$ chips.

The simulation results show that the carrier-to-noise ratio is 57dBHz and the accumulation time is 0.2ms. In Fig.4, the code correlation interval is half chip, that is, $d = 1$ and the accumulation time is 0.2ms.

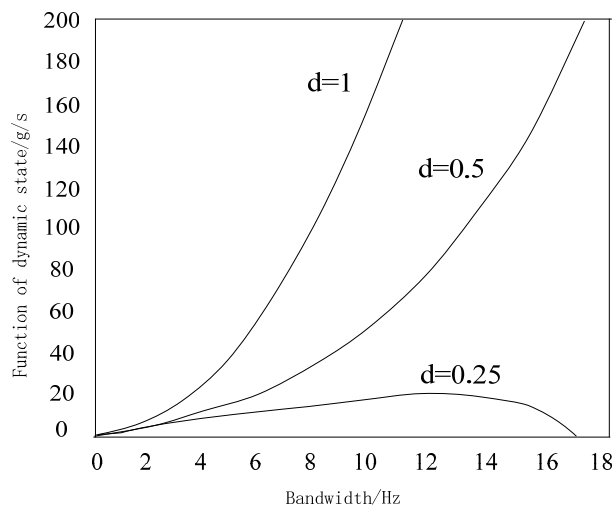


Figure 3. Effect of code-dependent intervals on tracking dynamic performance

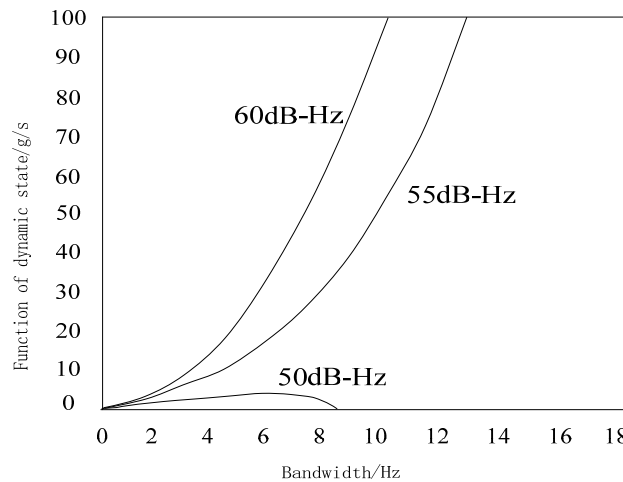


Figure 4. Effects of different carrier-to-noise ratios on tracking dynamic performance

It can be seen from Fig. 3 that for the case where the correlation interval is half a chip, the larger the correlation interval value is, the larger the linear region is, and the larger the traction range is, but the phase gain will decrease. Therefore, in order to make the traction capability and phase-sense traction range have the appropriate value, the code-dependent interval should be chosen in a trade-off. The code-dependent interval of the tracking in this paper is 0.25chip. As can be seen from Fig.4, the higher the carrier- The stronger the ability. When the signal-to-noise ratio is high, the dynamic performance of loop increases with the increase of bandwidth, which indicates that the

tracking error of noise is very small under the conditions of large SNR, which has a great influence on the dynamic performance of the loop. When the signal-to-noise ratio is low, the bandwidth increases and the SNR threshold of the tracking loop increases. Therefore, the tracking loop may lose its lock.

Summary

In this paper, the basic principles and tracking performance of delay-locked code tracking loop and composite carrier tracking loop are analyzed and the tracking algorithm used in this paper is determined: the phase of pseudo-code is precisely tracked by non-coherent delay code tracking loop. Finally, the correctness of the design algorithm is verified by simulation.

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