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Passivity-based Control of NPC Three-level Inverter

Shilan Shen [1, a], Qiu Hong [1,b] and Xiaofan Zhu [2,c]

[1] Guangzhou Power Supply, Guangzhou, Guangdong province, China

[2] School of Electrical Engineering, Wuhan University, Wuhan, Hubei province, China

343297505@qq.com [a], [b]hongqiu1983@126.com, [c] zxf8509@163.com

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Abstract. Unbalance of dc capacitor voltage is a key technical problem of NPC inverter. Through establishing the dc capacitor voltage balancing mathematical model of NPC three-level inverter, it can be proved that the NPC three-level inverter is a Passivity nonlinear system. By controlling the total charge of point injection is zero in a sampling period, and considering the Passivity dissipation characteristics of the nonlinear system, this paper calculated current of middle line and built up the passivity-based control model, and then kept the balance between voltages of dc capacitors, realized the low frequency current and dried the load transformer based on this. This control algorithm can achieve balance of dc voltages and output current at the same time, and the validity and feasibility of this control strategy is verified by simulation results, and very good effect has been proved by a practical engineering of 750kVA, NPC Three-level inverter. Based on this, a new idea of solving the unbalance of dc capacitor of diode clamped multi-level inverter is provided by this study.

Introduction

Multilevel inverters, which could increase the number of output voltage level and reduce the harmonic content of output, were suitable for high voltage and high power applications [1-3]. How to ensure the dc capacitor voltage balance was a key problem of the multilevel inverters controller, it could rise the harmonic content of output, cause voltage rise of switch devices and damage the inverters. With NPC (neutral-point-clamped) three-level inverter as an example, unbalance of dc capacitors could be solved from two ways, improving the hardware circuit or optimizing control algorithm. Improving the hardware circuit is increasing independent dc sources to dc capacitors, but it would cause system costs increasing, larger volume and complicated controller.

In the centerline of the NPC inverter alternating current was produced because that load current through bridge arm of each phase, and when the alternating current flowed into dc capacitors, corresponding voltage fluctuation would appear in dc capacitors. Besides, instantaneous unbalance current caused by disturbance might also make voltage deviation between two dc capacitors in the dynamic process. The passivity control could be used to achieve the purpose of the dc capacitors voltage balance by configuring the proper energy function, injecting suitable nonlinear damping and make two dc capacitors of NPC inverter voltage gradual convergence to half of the total dc voltage [4-6].

This paper changed NPC three-level inverter neutral voltage model to neutral current model, and designed voltage balance passivity control model of NPC three-level inverter capacitors based on the passivity theory. The positive-sequence component and the zero-sequence component of the reference voltage in the passivity control model would be calculated at the same time, so it would be easier to implement in engineering. The simulation show that passivity control algorithm can effectively balance control of dc voltage, keep good steady-state performance and fast dynamic response, and has simple algorithm and strong robustness. Effectiveness of the passivity control algorithm had been proved in 690V-750kVA engineering application.

Analysis of NPC three level inverter circuit and passivity control model

Circuit topology of NPC three level as shown in Figure 1: in this figure, u_{dc} is voltage of dc bus, in order to facilitate analysis, it was assumed that the u_{dc} is a constant; C_1 and C_2 are capacitance of dc capacitors, and C_1=C_2=C; u_{dc1} and u_{dc2} are voltages of dc capacitors; i_a, i_b, i_c are output currents of three phases ABC; u_{la}, u_{lb}, u_{lc} are voltages of load, O is the voltage neutral point, i_o is the total current of middle line; Q_1, Q_2, Q_3 and Q_4 are four IGBTs (Insulated Gate Bipolar Transistor) on bridge arm of phase A; D_1 and D_2 are clamping diodes on bridge arm of phase A; R_a, R_b, R_c are equivalent series loss resistances of three phases; L_{la}, L_{lb}, L_{lc} are equivalent series inductance of three phases. Conduction and shutoff of the IGBTs are controlled by SPWM(sine pulse width modulation).

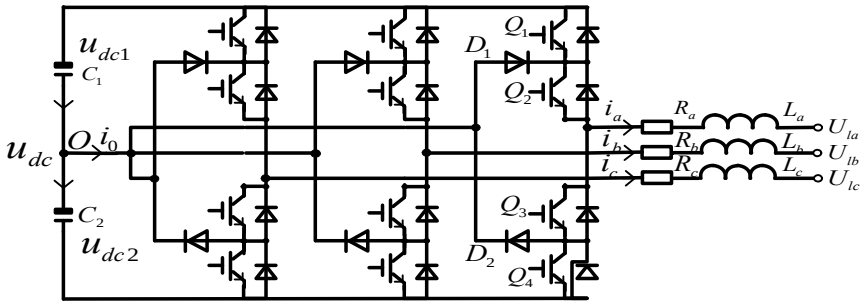


Fig. 1 *Main circuit topology of NPC*

Due to device different parameters, when energy was exchanging in the transient process, voltages of dc capacitors couldn't keep absolute equilibrium, what was called neutral-point offset. Neutral-point offset would cause harmonics output of NPC three-level inverter, impacting load performance, and if the imbalance was severe, devices of the NPC three-level inverter would be damaged.

If i_o=0, voltage of NPC dc capacitors will keep balance, however, only when the switch of NPC inverter is neutral point clamped, the current of middle line is not equal to zero, $i_o \neq 0$, so the current of middle line can be expressed as:

$$i_0 = [1-abs(S_a)]i_a + [1-abs(S_b)]i_b + [1-abs(S_c)]i_c = -abs(S_a)i_a - abs(S_b)i_b - abs(S_c)i_c \quad (1)$$

According to the principle of PWM control, the average output effect of the switch state would be the equivalent of reference voltage in a control cycle, signum function was defined as:

$$\mathrm{sgn}(u_x) = \begin{cases} 1 & ,u_x \geq 0 \\ -1 & ,u_x < 0 \end{cases} \quad (2)$$

Then the zero sequence voltage μ_0 that was need to stack could be got, with its constraint condition, in this formula, $u_{\max}$=max(u_a,u_b,u_c), $u_{\min}$=max(u_a,u_b,u_c) :

$$u_0 = -\frac{\mathrm{sgn}(u_a)\cdot u_{a1}\cdot i_a + \mathrm{sgn}(u_b)\cdot u_{b1}\cdot i_b + \mathrm{sgn}(u_c)\cdot u_{c1}\cdot i_c}{\mathrm{sgn}(u_a)\cdot i_a + \mathrm{sgn}(u_b)\cdot i_b + \mathrm{sgn}(u_c)\cdot i_c}, \quad \begin{cases} u_0 = 1-u_{\max}, & u_0 + u_{\max} > 1 \\ u_0 = -1-u_{\min}, & u_0 + u_{\min} < -1 \\ u_0 = u_0, ?(u_0 + u_{\max} \leq 1) \ \&? (u_0 + u_{\min} \geq -1) \end{cases} \quad (2)$$

The instruction output current of NPC three level inverter was supposed to $\boldsymbol{X}^* = \left[i_a^* \ i_b^* \ i_c^*\right]^T$, the actual output current was supposed to $\boldsymbol{X} = \left[i_a \ i_b \ i_c\right]^T$, the error output current was supposed to $\boldsymbol{X}_e = \left[i_{ae} \ i_{be} \ i_{ce}\right]^T$, and $\boldsymbol{X}^* = \boldsymbol{X} - \boldsymbol{X}_e$.

$$\boldsymbol{A}\dot{\boldsymbol{X}}_e + \boldsymbol{R}\boldsymbol{X}_e = \boldsymbol{F} - (\boldsymbol{A}\dot{\boldsymbol{X}}^* + \boldsymbol{R}\boldsymbol{X}^*) \quad (3)$$

In formula (3), $\boldsymbol{A} = diag\left[L_a \ \ L_b \ \ L_c\right]$ is a definite diagonal matrix, $\boldsymbol{R} = diag\left[R_a \ R_b \ R_c\right]$ is a definite symmetric matrix, which reflects the dissipation characteristics of the system,

$\boldsymbol{F}=[u_a-u_{la}, u_b-u_{lb}, u_c-u_{lc}, 0]^T$ is expression of exchanging energy between system and external environment, $\boldsymbol{Z}_f = diag[z_{fi}]$ (i=1,2,3) is damping coefficient matrix, the energy storage function is:

$$H=\frac{1}{2}\left(L_a i_{ae}^2+L_b i_{be}^2+L_c i_{ce}^2\right)=\frac{1}{2}X_e^T\boldsymbol{A}X_e \quad (4)$$

The derivative on both sides of the equation is: $\dot{H}=X_e^T\boldsymbol{A}\dot{X}_e=-X_e^T\left(\boldsymbol{R}+\boldsymbol{Z}_f\right)X_e\le W\left(X_e\right)<0$ (5)

In formula (5), $W\left(X_e\right)=-b\left\|X_e\right\|^2$, $b>0$, $\left\|X_e\right\|$ is Euclidean norms of X_e.

Above all, the error system is a under-actuated system, in an ideal world, i_a^*, i_b^*, i_c^* can be gradual tracking and $\Delta u_{dc12}^*=0$ at the same time.

$$\begin{cases} u_{a1}+u_0-u_{la}-\left(L_a\dfrac{di_a^*}{dt}+R_a i_a^*\right)+z_{fa}\left(i_a-i_a^*\right)=0 \\ u_{b1}+u_0-u_{lb}-\left(L_b\dfrac{di_b^*}{dt}+R_b i_b^*\right)+z_{fb}\left(i_b-i_b^*\right)=0 \\ u_{c1}+u_0-u_{lc}-\left(L_c\dfrac{di_c^*}{dt}+R_c i_c^*\right)+z_{fc}\left(i_c-i_c^*\right)=0 \\ u_0=-\dfrac{\mathrm{sgn}(u_a)\cdot u_{a1}\cdot i_a+\mathrm{sgn}(u_b)\cdot u_{b1}\cdot i_b+\mathrm{sgn}(u_c)\cdot u_{c1}\cdot i_c}{\mathrm{sgn}(u_a)\cdot i_a+\mathrm{sgn}(u_b)\cdot i_b+\mathrm{sgn}(u_c)\cdot i_c} \end{cases} \quad (6)$$

u_{a1}, u_{b1}, u_{c1} are the reference positive voltages of NPC three level inverter and u_0 is the zero sequence voltage needed to inject, that can be got by solving formula (6), then the passivity control block diagram of NPC three level inverter can be shown as figure 2.

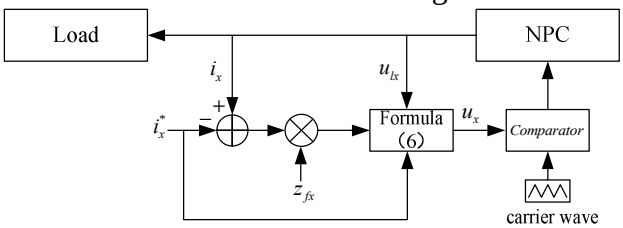


Fig. 2 *Passivity control block diagram of NPC*

Simulation and engineering test

In order to verify the NPC inverter under passivity control algorithm of the dynamic tracking performance and voltages of dc capacitors balancing effect, the simulation process is set to: in 0~0.3s, the operation process; in 0.3s~2s, instructions current (RMS) is 50A, frequency is 1Hz; in 2s~4s, instructions current change to 80A and the frequency reducing to 0.5Hz; In 4s~6s, instructions current increases to 80A and the frequency reducing to 0.2Hz.

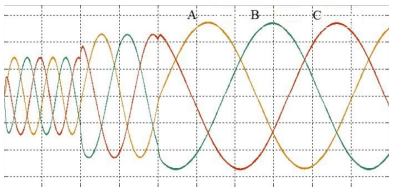


Fig. 3 *Three-phase currents*

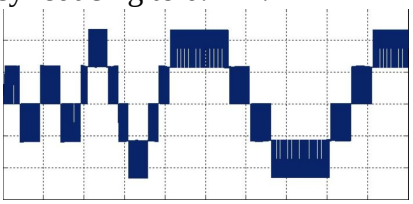


Fig. 4 *Line voltage* u_{ab}

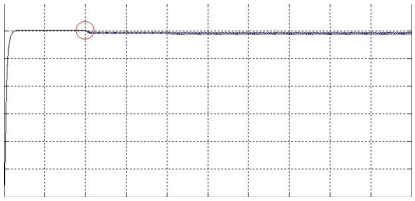
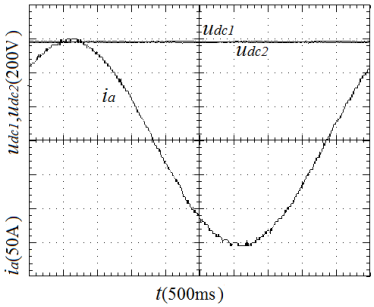


Fig. 5 *DC voltage* u_{dc1} *and* u_{dc2}

Figure 3 shows three-phase output current waveforms of NPC three-level inverter, figure 4 shows the line voltage waveform between phase A and phase B, figure 5 shows two voltage waveforms of dc capacitors u_{dc1} and u_{dc2}. From figure 3 to figure 5, the results show that when the instruction current

change, the output current of NPC three-level inverter is able to respond quickly and accurate tracking instruction current, and voltage deviation of two dc capacitors is less than 5 ‰.

Figure 6 shows A phase the output current waveform and two voltages waveform of dc capacitors from NPC three-level inverters, when instruction current is 60A and current frequency is 0.2 Hz, figure 7 shows the line voltage waveform between phase A and phase B, when instruction current is 110A and current frequency is 0.2 Hz.



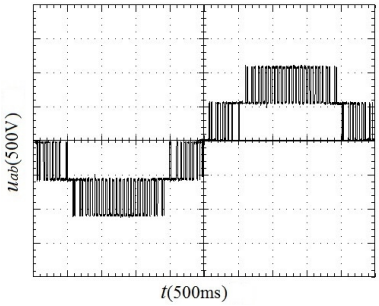


Fig. 6 *Output current and voltages of DC capacitors* **Fig. 7** *Line voltage between phase A and B*

From figure 6 and figure 7, the results show that the output current can follow instruction current and keep a good basic sinusoidal current waveform under passivity control, but because that dc side of NPC three-level inverter power supply capacity is limited, in, the voltage of dc capacitors produced a smaller decline when the instruction current of NPC three-level inverter increases.

Conclusion

Establishment of balance voltage of dc capacitors model and designing a passivity-based controller are to solve the problem of neutral-point offset in NPC three-level inverter, through theoretical derivation and simulation results, feasibility of the control algorithm was proved, and it can be achieved that the output current fast track the instruction current of different conditions, maintaining the balance between voltages of dc capacitors, and this passivity-based control algorithm can be applied to the diode clamping multilevel inverter.

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