

Response Analysis of Shunt Active Power Filter Under Various Line and Load Side Conditions

M. Shah and D. Nagotha

Institute of technology, Nirma University, Ahmedabad-382 481, India
{manisha.shah@nirmauni.ac.in ; 14meep18@nirmauni.ac.in}

Abstract: Solid state rectification of ac power using diodes and thyristors are drawing harmonic current and reactive power from ac supply and behave as non-linear load. During unbalancing of the three-phase supply voltage causes excessive neutral current, which results into low power factor, derating of equipment, poor efficiency and initiate triplen order harmonics. These all will raise serious issues related to power quality of the supply system. With the aim of mitigation of the same, the shunt active power filter is selected and analyzed with synchronous reference frame control algorithm. This paper mainly focuses on the performance analysis and simulation of shunt active power filter. The performance analysis of the filter in terms of reduction in %THD as per IEEE-519-1992 standard and unity power factor at line side for various dynamic conditions. Proposed scheme is simulated and validated in MATLAB/Simulink environment for various steady state and dynamic condition.

Keywords: *Active power filter, Harmonic mitigation, Power quality, Reactive power, %THD, Unity power factor*

1 Introduction

In recent year, harmonics pollution and reactive power compensation is a major issues of power quality because of the quick development of non-linear loads, as a part of modern applications in industries [1]. Because of present of harmonics and reactive power in the power system results to high transformer and power line losses, poor power factor, interference in the communication network system, reduced system stability, operation failure of electronic equipment and reduce safe operating margin [1,2,3]. Additionally, source voltage unbalance cause over excessive neutral current which leads to low power factor, derating of equipment, initiate the triplen order harmonics, and poor efficiency of the system [4].

Previously, Passive Power Filters (PPFs) was regularly used to unravel genuine harmonics and low power factor issues of the power system [5]. Hence, the PPFs is generally utilized as a part of the electrical field, because of the benefits of minimum cost, simple structure, and ease of use. However, the limitations of PPFs are: requirement of independent filter for each harmonic current or voltage, having limited filtering characteristics, impact brought on by parallel and series resonance between grid and filter impedance, large filter size, and selection the source inductance [5,6,7]. The Active Power Filters (APFs) turn out to be more famous as cure the weaknesses of the PPFs with real-time compensation [8]. In literature, for voltage harmonics compensation series active power filter and for current harmonics compensation shunt active power filter are examined with different control systems [7,8]. With the aim of mitigation of the current harmonics and solve other power quality issues of power system, the shunt active power filter (SAPF) is selected. The SAPF can compensate the load harmonic current without affecting the flow of the fundamental source current. The working principle of SAPF is harmonics current generator, which feed harmonics current 180° out of phase at the Point of Common Coupling (PCC) for elimination of current harmonics presence in the power grid [8,9,10]. So, that the SAPF provides effective compensation characteristics.

In this paper, the SAPF is proposed to meet the need of current harmonic suppression and power factor improvement with synchronous reference frame (SRF) control algorithm. It is a desirable feature of any closed loop control system to adjust with the varying load condition with typical limitation in overshoot and settling period. Also, under unbalanced voltage source, this has been tested with adopted closed loop control technique for power factor improvement and harmonic elimination. This paper establishes closed loop simulation model of SAPF in MATLAB/Simulink environment for various steady state and dynamic condition at load and line sides.

2 The Shunt Active Power Filter

The shunt active power filter session includes main power circuit, detecting harmonic current algorithm, PWM technique used for generation of switching signals as an inner current controlled loop and controlling of dc bus voltage of two-level PWM inverter as outer voltage control loop.

2.1 Main Power Circuit

The main power circuit diagram of the shunt active power filter is shown in Fig.1. The three-phase, 400 V, 50 Hz ac supply connected to the three-phase diode bridge rectifier i.e. non-linear load through source inductance (L_s) and load side inductance (L_{ac}). The active power filter is connected in parallel to the power lines at PCC through coupling inductor (L_c). The value estimation of the coupling inductor results in to filtering of the high frequencies noise produced by the switching of the power converter and permitting high di/dt on the inductor to take after the harmonics current should be reduced [11]. The SAPF is a two-level PWM voltage source inverter supplied by a capacitor (C_{dc}) and controlled by hysteresis current controller. The inductance L_{ac} should be design too much larger in size than the inductance L_s , in order to shortcoming current streaming into the rectifier [12].

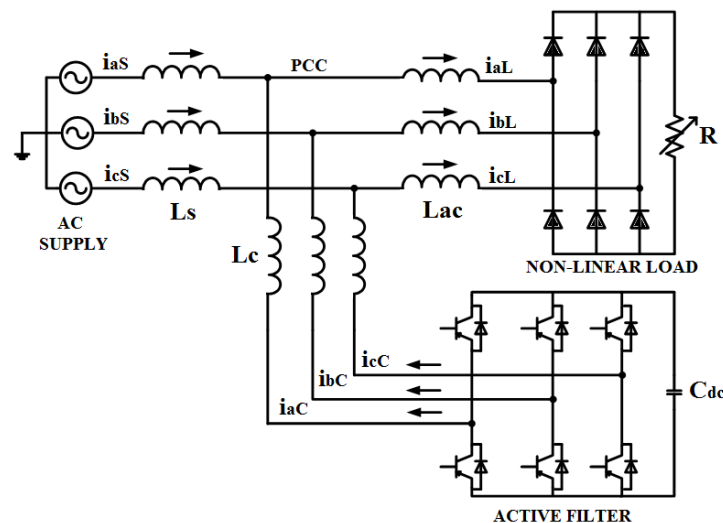


Fig.1 The scheme of main power circuit of SAPF

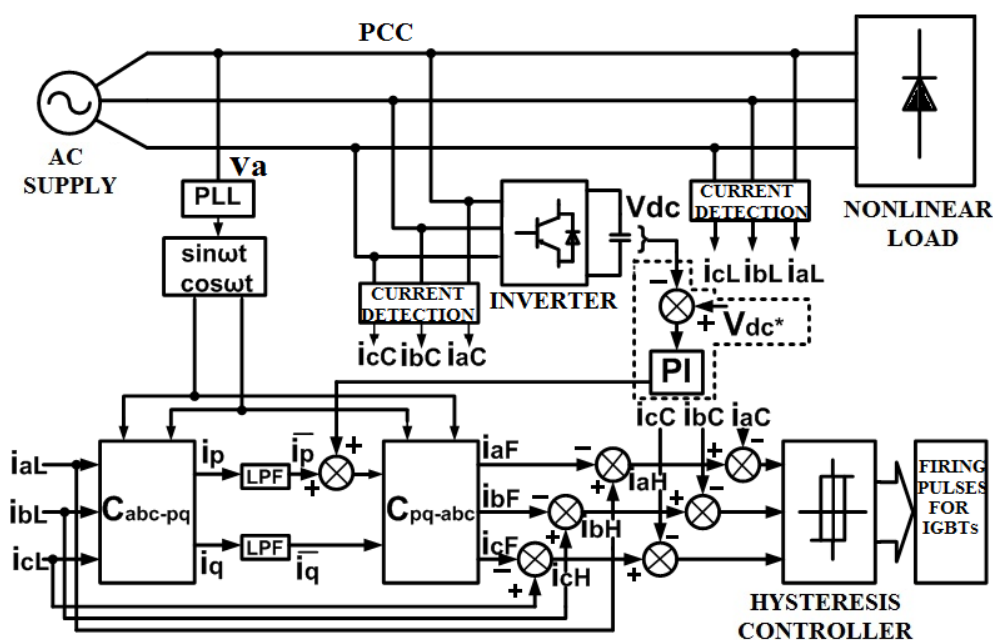


Fig.2 Block diagram of SRF algorithm

2.2 Synchronous Reference Frame

In this paper, the synchronous reference frame (SRF) algorithm is used for reference harmonic current generation. This theory will calculate reference signals of voltage and current in rotating reference frame not at all like p-q theory [10,13,14]. Fig.2 shows block diagram of the harmonics current detecting SRF algorithm. Adopted SRF algorithm with phase locked loop (PLL) circuit for reference compensating current generation, which precisely distinguishes the active and reactive current components of the fundamental positive sequence of the nonlinear and unbalanced load currents under the balance and unbalance of supply voltage [10]. A sinusoidal supply voltage of phase-A (V_a) is applied to PLL circuit for measurement of phase angle and frequency of the fundamental positive sequence voltage component. Initially, Fig.2 shows the transformation the instantaneous three-phase load current (i_{aL}, i_{bL}, i_{cL}) to the fundamental instantaneous active and reactive power current (i_p, i_q) by using transformation matrix C_{abc-pq} . It consists of both α - β co-ordinate through Clark's transformation matrix and in d-q co-ordinate with ωt angular velocity by rotating co-ordinate transformation matrix is given by equation (1) [10].

$$\begin{aligned} \begin{bmatrix} i_p \\ i_q \end{bmatrix} &= \sqrt{2/3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} \sin\omega t & -\cos\omega t \\ -\cos\omega t & -\sin\omega t \end{bmatrix} \begin{bmatrix} i_{aL} \\ i_{bL} \\ i_{cL} \end{bmatrix} \\ &= \sqrt{2/3} \begin{bmatrix} \sin\omega t & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ -\cos\omega t & -\cos(\omega t - \frac{2\pi}{3}) & -\cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} i_{aL} \\ i_{bL} \\ i_{cL} \end{bmatrix} \\ &= C_{abc-pq} \begin{bmatrix} i_{aL} \\ i_{bL} \\ i_{cL} \end{bmatrix} \end{aligned} \quad (1)$$

$$\begin{aligned} \begin{bmatrix} i_{aF} \\ i_{bF} \\ i_{cF} \end{bmatrix} &= \sqrt{2/3} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} \sin\omega t & -\cos\omega t \\ -\cos\omega t & -\sin\omega t \end{bmatrix} \begin{bmatrix} \bar{i}_p \\ \bar{i}_q \end{bmatrix} \\ &= \sqrt{2/3} \begin{bmatrix} \sin\omega t & -\cos\omega t \\ \sin(\omega t - \frac{2\pi}{3}) & -\cos(\omega t - \frac{2\pi}{3}) \\ \sin(\omega t + \frac{2\pi}{3}) & -\cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} \bar{i}_p \\ \bar{i}_q \end{bmatrix} \\ &= C_{pq-abc} \begin{bmatrix} \bar{i}_p \\ \bar{i}_q \end{bmatrix} \end{aligned} \quad (2)$$

The active power current (i_p) and reactive power current (i_q) are composed of DC component and oscillating component. Now, by using Low Pass Filter (LPF) the oscillating components from both currents are eliminated and the average value of active power current component (\bar{i}_p) and reactive power current component (\bar{i}_q) are obtained. By applying inverse d-q co-ordinate transformation matrix and inverse Clark's transformation matrix i.e. C_{pq-abc} , the fundamental current (i_{aF}, i_{bF}, i_{cF}) is obtained by given equation (2) [10]. Finally, the fundamental currents are compared with the load currents, and the reference harmonics current (i_{aH}, i_{bH}, i_{cH}) is given by equation (3) [10].

$$\begin{bmatrix} i_{aH} \\ i_{bH} \\ i_{cH} \end{bmatrix} = \begin{bmatrix} i_{aL} \\ i_{bL} \\ i_{cL} \end{bmatrix} - \begin{bmatrix} i_{aF} \\ i_{bF} \\ i_{cF} \end{bmatrix} \quad (3)$$

2.3 Hysteresis Current Controller

The fixed-band hysteresis current controller is implemented for SAPF as an inner current controlled loop. It is used in each phase independently and generates the switching signals for the PWM voltage source two-level inverter. The present current controller strategy delivers on reference current to shape the upper and lower points of confinement of a fixed hysteresis band (Band limit: 1 A and -1 A) [15]. Fig.3 illustrates that actual compensating current (i_{xH}) is compared with reference harmonics current (i_{xH}), (where $x = a, b, c$) and resulting error is given to hysteresis controller to determine gating signals for the inverter. The advantages of fixed band- HCC

are simple design and unconditioned stability [15]. However, due to the lake of co-ordination between the phases causes random switching frequency and overshooting of the current.

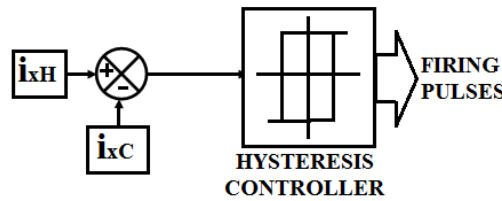


Fig.3 Hysteresis current controller

2.4 DC Bus Voltage Control

A DC bus voltage controller is utilized to control dc voltage (V_{dc}) and compensate the PWM-inverter losses [1,16]. This controller is generally PI (Proportional-Integral) controller to control the voltage across the capacitor (C_{dc}). The measured dc bus voltage (V_{dc}) across the capacitor (C_{dc}) is compare with reference DC voltage (V_{dc}^*), then resulting error is applied to a Proportional-Integral (PI) controller. The output of PI controller would be superimposing on \bar{i}_p , so that output reference harmonics current (i_{aH}, i_{bH}, i_{cH}) generated by the SRF algorithm having the information of the voltage across the capacitor (Refer Fig. 2).

3 Simulation Results Analysis of SAPF

In order to verify the compensation characteristics and performance of the SAPF under fixed load, dynamic load and unbalance supply voltage, the simulation model of the system is created in MATLAB/Simulink environment. The non-linear load is a three-phase six-pulse diode rectifier with a resistive load. The simulation design parameters are given in table 1.

Table 1. SAPF DESIGN PERAMETERS

Source and Load		SAPF	
V_s	400 v	V_{dc}	600 v
f_s	50 Hz	C_{dc}	4500 μF
L_s	0.1 mH	L_c	1 mH
L_{ac}	1.5 mH	Two-level IGBT Converter	
R	10 Ω	Hysteresis band 2 A	
(Fixed Load)		(Current controller)	
$R_1 = 10 \Omega, R_2 = 5 \Omega$		PI controller Yes	
(Dynamic Load)		(DC voltage controller)	

3.1 Analysis with Fixed Load

The simulation results waveforms are shown in Fig. 4 for phase-A under 600V dc bus voltage with fixed value of R load. Fig. 4(a) shows the phase-A load current (i_{aL}) without compensation, the shape of load current is non-sinusoidal due to the use of non-linear load. It consist of both fundamental and harmonics current components. Fig. 4(b) shows the phase-A source current (i_{aS}) waveform after compensation of harmonics using SAPF. This is sinusoidal in shape due to elimination of harmonics after compensation. Fig. 4(c) is the actual compensating current (i_{aC}) coming out from the two-level voltage source PWM inverter supplied to the PCC. Fig. 4(d) is the single phase-A voltage and current which shows the distortion power factor is improved and hence the total power factor is unity. The waveforms shown in the Fig.4 remain same for the phase-B and phase-C with 120° and 240° phase shift respectively with respect to phase-A.

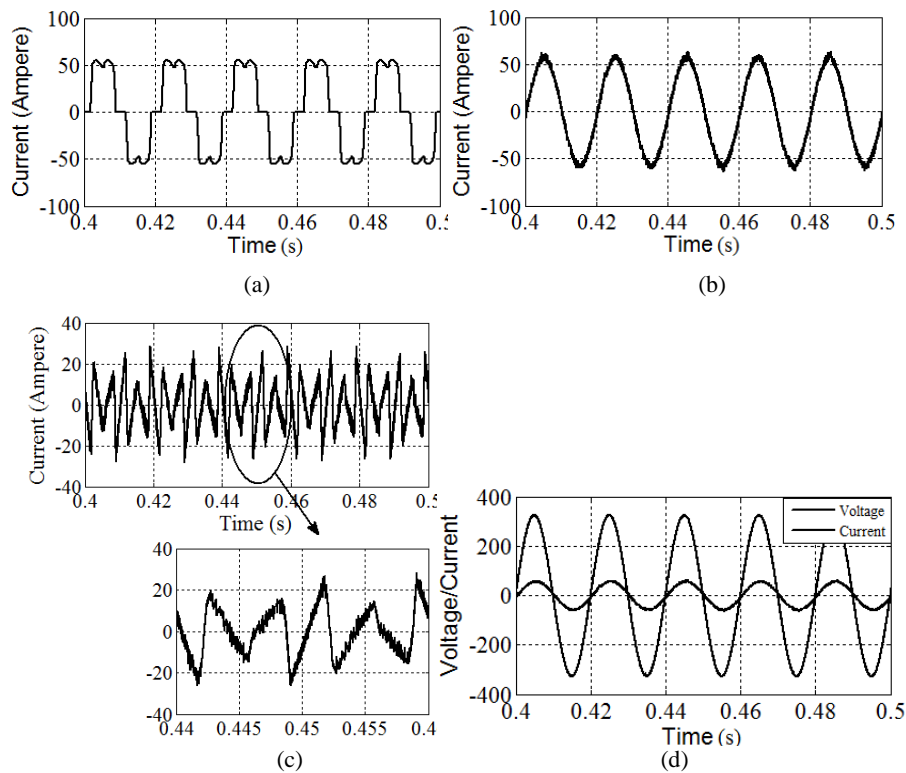


Fig.4 Simulation result with fixed R load (a) Phase-A load current without compensation, (b) phase-A source current with compensation, (c) phase-A compensating current, (d) Phase-A voltage and current.

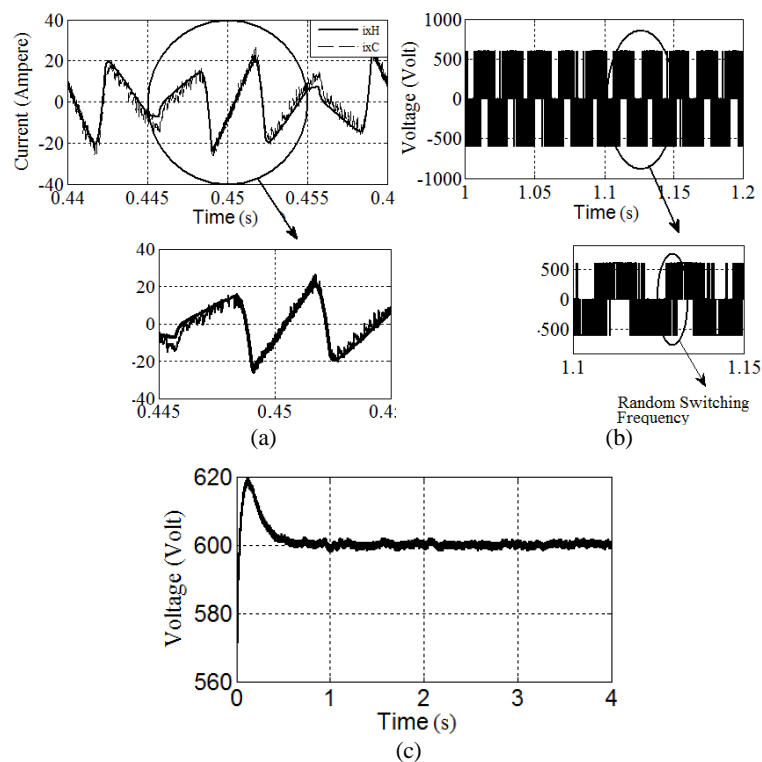


Fig.5 Simulation results (a) reference (i_{aH}) and actual (i_{xC}) compensating currents of phase-A (b) line to line voltage of inverter (c) DC bus voltage of inverter

As discussed above about hysteresis current controller (HCC) is used for obtained the gate pulses for controlling the IGBTs used in two-level PWM inverter. As shown in Fig. 5(a), the actual compensating currents (i_{xC}) exactly tracking the reference harmonics current (i_{xH}) because of set upper and lower band limit of hysteresis band. Also the line to line voltage of the two-level PWM inverter is shown in Fig. 5(b), which shows the hysteresis current controller gives the random switching of voltage vector, which is due to the lake of coordination between the phases. Under the fixed value of resistive load, the simulation results of DC bus voltage is shown in Fig. 5(c). Seen from the DC voltage across the capacitor can rapidly stable inside time (t) = 0.4 second and follow the reference voltage because of utilization the PI controller as external voltage controlled loop.

The performance analysis of the three-phase source current waveform by using Fast Fourier Transform (FFT). The FFT curve of the load current without compensation is shown in Fig. 6(a). After the stability of DC bus voltage and compensation of harmonics present in grid, the FFT curve of source or grid current is shown in Fig. 6(b). From the simulation waveforms the control algorithm has successfully been obtained the compensation according to IEEE-519 standard for source current under fixed load.

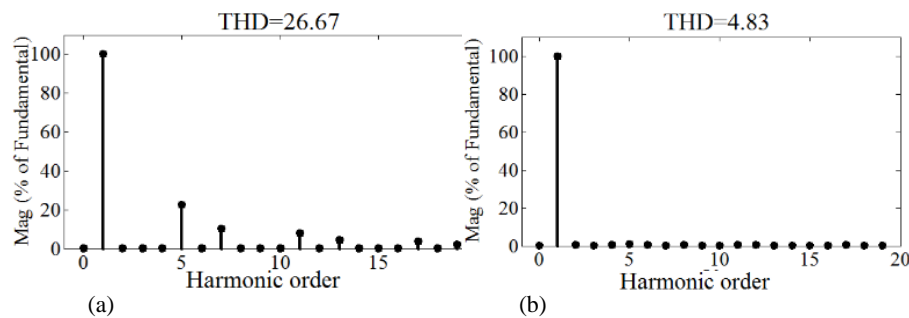
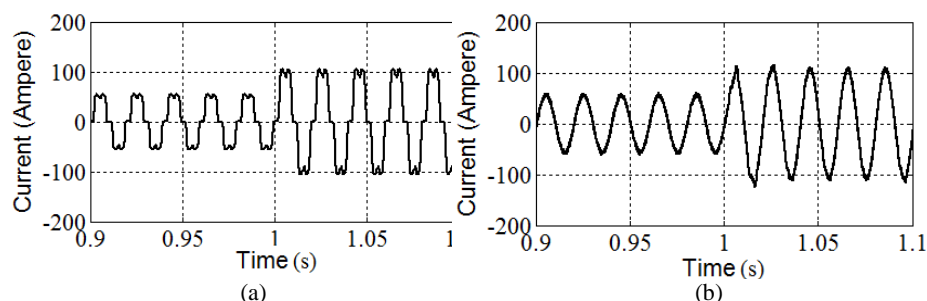


Fig.6 FFT curves (a) FFT of load current without compensation (b) the FFT of Source current with compensation

3.2 Analysis with Dynamic Load

In real power system, the variation of load may occur. The simulation waveforms are shown in Fig.7 under 600V DC bus voltage with nonlinear load varies from R_1 to R_2 at time (t) = 1 sec. The source current harmonics are increases at t = 1 sec., yet the remuneration impact can recoup quickly. Fig. 10(a) is the phase-A load current (i_{aL}) waveform without compensation, Fig. 10(b) is the phase-A source current (i_{aS}) waveform after compensation of harmonics present in the grid by SAPF, Fig. 10(c) is the actual compensating current (i_{aC}) coming out from the inverter used in the SAPF. Fig. 10(d) is the DC bus voltage across the capacitor. Fig. 10(e) is one phase-A voltage and current waveforms. The waveforms shown in the Fig.10 will remain same for the phase-B and phase-C with 120° and 240° phase shift respectively with respect to phase-A.

The performance analysis of three-phase source current of the grid use FFT. Under dynamic load condition, the FFT spectrum of line current before compensation and after compensation of harmonics are shown in Fig. 8(a) and Fig. 8(b) respectively. The %THD of grid current reduced from 22.52% to 3.80%. Subsequently, from the simulation results the control algorithm has been effectively acquired the compensation of grid current under dynamic loading condition.



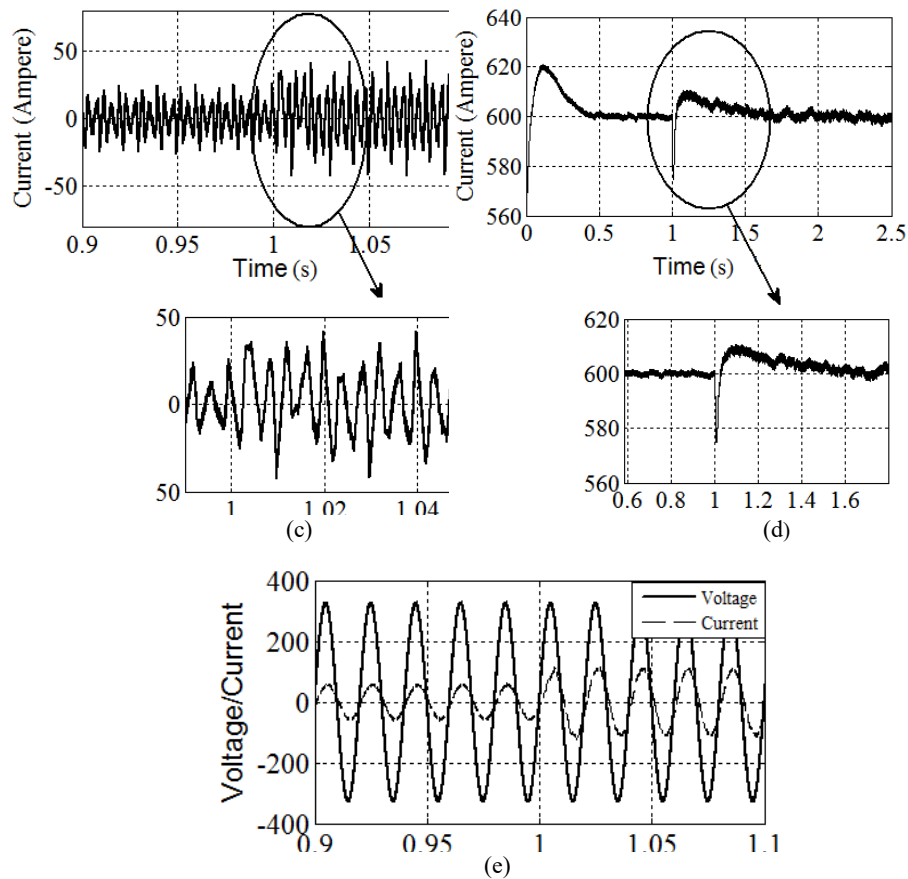


Fig.7. Simulation results with dynamic R load (a) phase-A load current without compensation, (b) Phase-A source current with compensation, (c) Phase-A actual compensating current, (d) DC bus voltage, (e) Phase-A voltage and Current.

3.3 Analysis with Unbalance Source Voltage

In actual power system the unbalancing of source voltage may occurs and causes the flow of excessive neutral current. Hence, the triplen order harmonic component is introduced in the supply system. Also the power factor and efficiency of the system will be poorer rather than the balance supply voltage. So, the SAPF can be used to balance the source current and compensate the harmonics. Fig.9 shows the simulation results of SAPF with unbalance source voltage and fixed value of R-load. Fig. 9(a) is the unbalance source voltage supplies to non-linear load. Here, phase-C voltage reduced from 400 V to 320 V (20% of line to line voltage). Fig.14 (b) shows the load current without compensation, the phase-C current magnitude is reduced due to its reduction in phase voltage. Fig.14 (c) shows the three-phase balance source current with compensation, it represents the SAPF can eliminate all triplen order harmonics from the source current. Fig. 14 (d) shows the phase-A voltage and current waveform, it represents the SAPF can improve the overall power factor to be unity. The harmonic spectrum of phase-A and C line current without and with compensation are shown in Fig. 10 and Fig. 11 respectively. The phase-B FFT spectrum is similar to the phase-A.

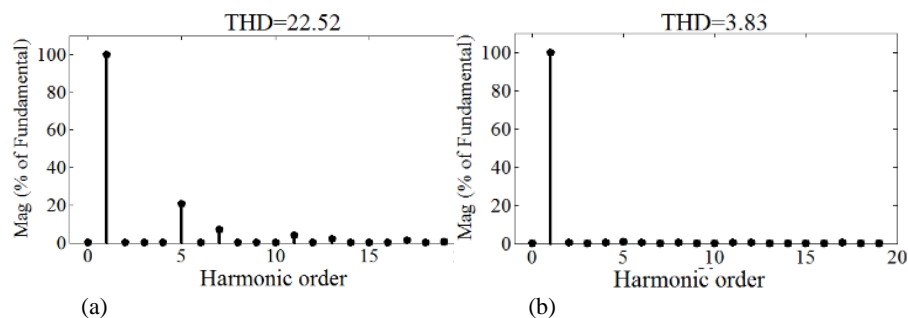


Fig.8 FFT curve (a) FFT of load current under variable load without compensation, (b) FFT of source current under variable load with compensation

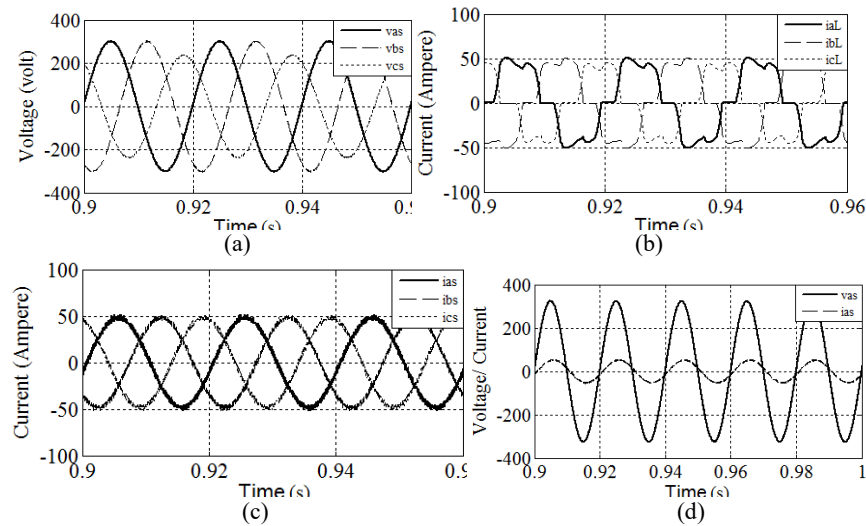


Fig.9 Simulation results with unbalance source voltage (a) Three-phase unbalance source voltage (b) Three-phase load current without compensation (c) Three-phase balance source current with compensation (d) Phase-A voltage and current

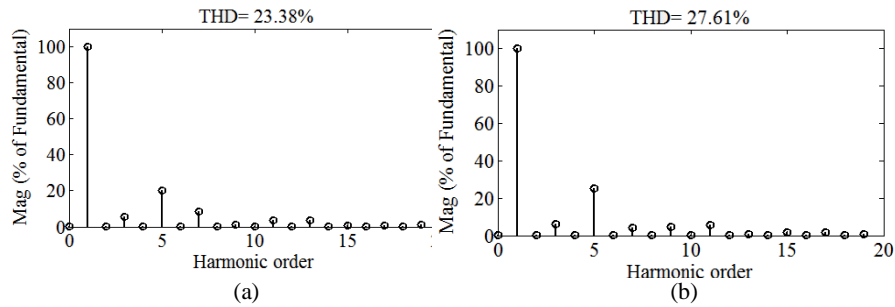


Fig.10 Harmonic spectrum of load currents (a) phase-A load current without compensation (b) phase-C load current without compensation

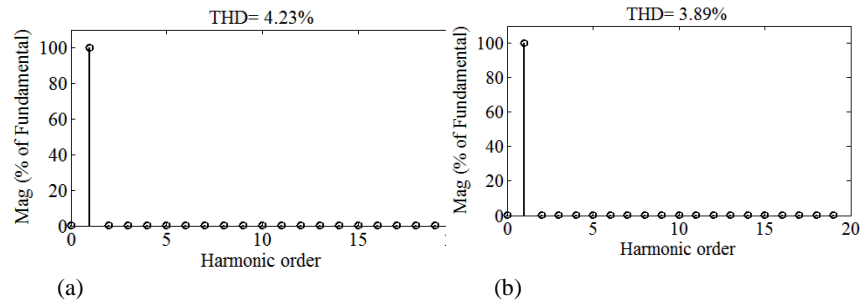


Fig.11 harmonic spectrum of source currents (a) phase-A source current with compensation (b) phase-C source current with compensation

4 Conclusion

Simulation and performance analysis of shunt active power filter (SAPF) with fixed load, dynamic load and unbalance source voltage is presented in this paper. It has been observed that proposed controller is able to mitigate the harmonics in line current and provide unity power factor with %THD less than 5% as per IEEE-519-1992 under all under steady state and dynamic conditions at load side and line side, which proves the robustness of the proposed controller.

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