A Two-dimensional Analytical Model and Simulation for Dual Material Gate Junctionless Transistor

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Abstract. To investigate the short channel effect for Dual Material Gate Silicon on Insulator junction-less Transistor (DMG SOI JLT) of a two dimensional channel potential model is developed. This model is validated by simulation (COGENDA Visual TCAD) result. It has been observed that for a junction-less transistor with Dual Material Gate (DMG) current driving capability improves secondly, channel potential step function that results drain voltage variation do not affect on barrier between source and channel due to the work function difference of the gate material. This increase in current driving capability increases and hot electron effect, Drain induced barrier lowering problem and reduces its dual material different work function structure.

Keywords: ***Dual Material Gate (DMG); two-dimensional (2-D) modeling; silicon-on-insulator (SOI) MOSFET; Short channel effects (SCEs).***

1 Introduction

The conventional metal oxide semiconductor field effect transistor suffers with problem of short channel effect, SCE, because channel length reduces as according International Technological Roadmap (ITRS) size of transistor is shrinking. However, due to this gate controllability on channel reduces and drain works as another gate. SCEs gives-up a hot electron effect, threshold voltage roll-off, Drain induced barrier lowering and on and off current ratio.

A very small channel thickness and fully depleted silicon on insulator MOSFET with no latch up problem, very less junction capacitance, more current driving capability due to improved channel mobility and SCEs[1]. Recently a transistor without P-N junction but with uniformly doped channel region by same material has better SCE performance, resulting in simplified process flow, low thermal budget and low power & high performance [2],[3].[4],[5]. Presently, MOS transistor enters in nanometer regime with maximum high doping density gradients required for formation of P N junctions. A very high doping atoms concentration impurity diffusion in semiconductor material and formation of ultra-shallow junctions is technological challenge in semiconductor industry. The recently proposed junction-less transistor has no conventional source and drains junction and are uniform distribution through source, channel and drain region and have been experimentally demonstrated [6],[7],[8].

M. Jagdesh Kumar et.al demonstrated and design a novel structure Dual Material Gate SOI MOSFET having two dimensional surface potential model and achieved improved Drain Induced Barrier Lowering (DIBL), hot electron effect and current driving capability due to different work function of different material gate.[2], however, junction-less transistor suffers from very less current driving capability due to very high doping concentration [9],[10],[11]. Dual material gate junction-less MOSFET is a best candidate for suppressing short channel effect in nanoscale regime. Hougin Lou demonstrate Dual Material Gate junctionless nanowire transistor and results shows the improvement in the performance for trans-conductance, cut off frequency and output conductance compared to single material gate junctionless nanowire transistor. Authors could not get literature for two dimensional analytical model of Dual Material Gate Silicon on Insulator junction-less transistor (DMG SOI JLT), which plays important role in CMOS chip design. In this article two dimensional analytical bulk potential models is design for fully depleted DMG SOI junction-less MOSFET using Poisson equation has been studied. Channel potential is evaluated by its model and observed results for DIBL, hot electron effect and current driving capability, it gives improvement because no vertical electric field on the channel in junctionless transistor and are verified with simulation result of COGEND visual TCAD.

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2 Two-Dimensional Bulk Potential Model

Device structure n-type Dual Material Gate SOI junction-less Transistor is shown in Fig.1. In this Polysilicon p^+ as a gate material and uniform doping for the source, drain and channel region. A DMG SOI JLT has two metal gates M_1 and M_2 with Gate M_1 work function has greater than gate M_2 [3].

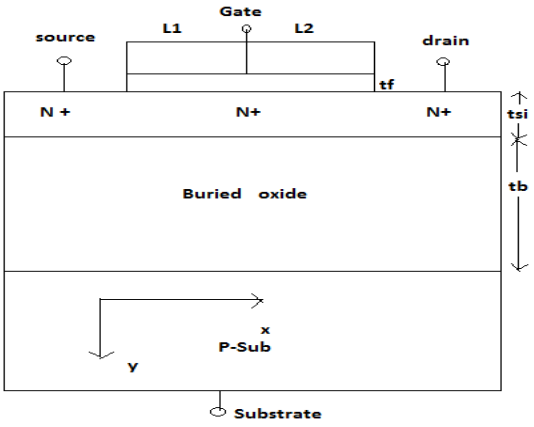

Fig-1: Novel structure of n-channel DMG SOI Junctionless Transistor.

Fig-1 shows n-channel Dual Material Gate silicon on insulator junction-less transistor with uniform doping N_D ($0.4x10^{18}$ cm^{-3}) through source, channel and drain region. Channel thickness 10nm, buried oxide 360nm, channel length 40nm and oxide thickness 1nm [3].

2-D Poisson equation for n-channel DMG SOI JLT (channel assume fully depleted)

$$\frac{d^2\Phi(x,y)}{dx^2}+\frac{d^2\Phi(x,y)}{dy^2}=\frac{-qN_D}{\varepsilon_{si}} \quad for 0\le x\le L, 0\le y\le tsi \tag{1}$$

Where

N_D is doping density
ϵ_{si} is permittivity of channel region
q is electron charge
$\Phi(x, y)$ is potential distribution [1].

$$\Phi(x,y)=\Phi_s(x)+C_1(x)y+C_2(x)y^2 \tag{2}$$

$\Phi_s(x)$ is surface potential
$C_1(x)$ and $C_2(x)$ is arbitrary coefficient.

In this structure gate is split into two parts M_1 and M_2 and potential distribution under M_1 and M_2 can be written as,

$$\Phi_1(x,y)=\Phi_{s1}(x)+C_{11}(x)y+C_{12}(x)y^2$$

$$0\le x\le L_1, 0\le y\le t_{si} \tag{3}$$

$$\Phi_2(x,y)=\Phi_{s2}(x)+C_{21}(x)y+C_{22}(x)y^2$$

$$0\le x\le L_1+L_2, 0\le y\le t_{si} \tag{4}$$

1) Electric flux distribution at gate M_1 and M_2.

$$\left.\frac{d\Phi_1(x,y)}{dy}\right|_{y=0}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\Phi s_1(x)-V_{GS_1}}{tf} \quad \text{for Metal 1} \tag{5}$$

$$\frac{d\Phi_1(x,y)}{dy}_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\Phi s_2(x) - V_{GS_2}{}^1}{tf} \quad \text{for metal 2} \tag{6}$$

Where

ε_{ox} is dielectric constant

t_f is gate oxide thickness.

$$V_{GS_1}{}^1 = V_{GS} - V_{FB_1}$$

$$V_{GS_2}{}^1 = V_{GS} - V_{FB_2}$$

where V_{GS1} and V_{GS2} gate voltage and V_{FB1} and V_{FB2} flat band voltage at gate1 and gate2 respectively.

2) Electric flux at buried oxide for metal gate M_1 and M_2 respectively.

$$\frac{d\Phi_1(x,y)}{dy}_{y=tsi} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V_{SUB}{}^1 - \Phi_B(x)}{tb} \quad \text{for metal 1} \tag{7}$$

$$\frac{d\Phi_2(x,y)}{dy}_{y=tsi} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V_{SUB}{}^1 - \Phi_B(x)}{tb} \quad \text{for metal 2} \tag{8}$$

t_b is buried oxide thickness and Φ_B is back potential at buried channel interface.

$$V_{SUB}{}^1 = V_{SUB} - V_{FB,b}$$

V_{SUB}=substrate bias

$V_{FB,b}$= back channel flat band voltage.

3) Surface potential is continuous at two dissimilar metal gate1 and gate2.

$$\Phi_1(L_1, 0) = \Phi_2(L_1, 0) \tag{9}$$

4) Electric field is continuous at two dissimilar metal gate1 and gate2.

$$\frac{d\Phi_1(x,y)}{dx}|_{x=L_1} = \frac{d\Phi_2(x,y)}{dx}|_{x=L_1} \tag{10}$$

5) The potential at source side is V_{bi}

$$\Phi_1(0, 0) = \Phi_{s1}(0) = V_{bi} \tag{11}$$

6) The Potential at drain side is $V_{bi}+V_{ds}$

$$\Phi_2(L_1+L_2, 0) = \Phi_{S2}(L_1+L_2) = V_{bi}+V_{ds} \tag{12}$$

Built in potential

$$V_{bi} = \frac{KT}{q} \log_e \frac{N_D}{n_i^2} \tag{13}$$

Under Metal1 from (3),(5) &(7) we get

$$\Phi_1(x,y) = \Phi_{s1}(x) + C_{11}(x)y + C_{12}(x)y^2$$

$$\frac{d\Phi_1(x,y)}{dy}|_{y=0} = 0 + C_{11}(x) + 2C_{12}(x)y$$

$$C_{11}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\Phi_{s1}(x) - V_{GS1}{}^1}{tf} \tag{14}$$

$$\Phi_{S1}(x) + C_{11}(x)tsi + C_{12}(x)tsi^2 = \Phi_B(x)$$

$$C_{11}(x) + 2C_{12}(x)tsi = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V_{SUB}^1 - \Phi_B(x)}{tb}$$

$$C_{12} = C_b\left(\frac{V_{SUB}^1 - \Phi_{B(x)}}{tb}\right) \tag{15}$$

$$C_b = \frac{\varepsilon_{ox}}{tf}$$

Similarly for metal2 obtain following expression using (4),(6) &(8)

$$\Phi_{S2}(x) + C_{21}(x)tsi + C_{22}(x)tsi^2 = \Phi_{B(x)} \tag{16}$$

$$C_{21} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\Phi_{S2}(x) - V_{GS2}^1}{tf}$$

Region under metal 1, Solving (13)-(15) for $C_{12}(x)$

$$C_{12(x)} = \frac{V_{SUB}^1 + V_{GS1}^1\left(\frac{c_f}{c_b} + \frac{c_f}{c_{si}}\right) - \Phi_{S1}(x)\left[1 + \frac{c_f}{c_b} + \frac{c_f}{c_{si}}\right]}{t_{si}^2\left(1 + 2\frac{c_{si}}{c_b}\right)}$$

$$C_b = \frac{\varepsilon_{OX}}{t_b}, C_{si} = \frac{\varepsilon_{si}}{t_{si}}$$

Substituting $C_{11}(x)$ and $C_{12}(x)$ values in (3) and obtain potential distribution when $\Phi_1(x,y)$ in (1)

$$\frac{d^2\Phi_{s1}(x)}{dx^2} - \alpha\Phi_{s1(x)} = \beta_1 \tag{17}$$

$$\frac{d^2\Phi_{S2(X)}}{dx^2} - \alpha\Phi_{S2}(x) = \beta_1$$

$$\alpha = \frac{2\left(1 + \frac{C_f}{C_b} + \frac{C_f}{C_{si}}\right)}{t_{si}^2\left(1 + 2\frac{C_{si}}{C_b}\right)}$$

$$\beta_1 = \frac{-qN_D}{\varepsilon_{si}} - 2V_{GS1}^1\left(\frac{\frac{C_f}{C_b} + \frac{C_f}{C_{si}}}{t_{si}^2\left(1 + 2\frac{C_{si}}{C_b}\right)}\right) - 2V_{SUB}^1\left[\frac{1}{t_{si}^2\left(1 + 2\frac{C_{si}}{C_b}\right)}\right]$$

$$\beta_2 = \frac{-qN_D}{\varepsilon_{si}} - 2V_{GS2}^1 \left(\frac{\frac{C_f}{C_b} + \frac{C_f}{C_{si}}}{t_{si}^2 \left(1 + 2\frac{C_{si}}{C_b} \right)} \right) - 2V_{SUB}^1 \left[\frac{1}{t_{si}^2 \left(1 + 2\frac{C_{si}}{C_b} \right)} \right]$$

Above β_1 and β_2 differential equation

$$\Phi_{S1}(x) = A\exp(\lambda_1 x) + B\exp(\lambda_2 x) - \frac{\beta_1}{\alpha}$$

$$\Phi_{S2}(x) = C\exp\left(\lambda_1 (x - L_1)\right) + D\exp\left(\lambda_2 (x - L_1)\right) - \frac{\beta_2}{\alpha}$$

Where

$\lambda_1 = \sqrt{\alpha}$ and $\lambda_2 = -\sqrt{\alpha}$ .Now using boundary condition (9)-(12) to solve for A,B,C,D where $\sigma_1 = -\beta_1/\alpha$ and $\sigma_2 = -\beta_2/\alpha$.

$$C = A\exp(\lambda_1 L_1) + \frac{\sigma_1 - \sigma_2}{2}$$

Through the channel electron driving capability depends on electric field. Electric field along the x-direction under gate M_1 and M_2 is given as.

$$E_1(x) = \frac{d\Phi_1(x,y)}{dx}_{y=0} = \frac{d\Phi_{s_1}(x)}{dx} = A\lambda_1 \exp(\lambda_1 x) + B\lambda_2 \exp(\lambda_2 x) \tag{18}$$

$$E_2(x) = \frac{d\Phi_2(x,y)}{dx}_{y=0} = \frac{d\Phi_{s_2}(x)}{dx} = C\lambda_1 \exp(\lambda_1 (x - L_1)) + D\lambda_2 \exp(\lambda_2 (x - L_1)) \tag{19}$$

$$A = \frac{(V_{bi} - \sigma_2 + V_{DS})\exp\left(-\lambda_1 (L_1 + L_2)\right)}{1 - \exp\left(-2\lambda_1 (L_1 + L_2)\right)} - \frac{\exp\left(-\lambda_1 (L_1 + L_2)\right)(V_{bi} - \sigma_1) \times \exp\left(-\lambda_1 (L_1 + L_2)\right)}{1 - \exp\left(-2\lambda_1 (L_1 + L_2)\right)} - \frac{(\sigma_1 - \sigma_2)\cosh(\lambda_1 L_2) \times \exp\left(-\lambda_1 (L_1 + L_2)\right)}{1 - \exp\left(-2\lambda_1 (L_1 + L_2)\right)}$$

$$B = \frac{(V_{bi} - \sigma_1)}{1 - \exp\left(-2\lambda_1 (L_1 + L_2)\right)} - \frac{(V_{bi} - \sigma_2 + V_{DS})\exp\left(-\lambda_1 (L_1 + L_2)\right)}{1 - \exp\left(-2\lambda_1 (L_1 + L_2)\right)} + \frac{(\sigma_1 - \sigma_2)\cosh(\lambda_1 L_2)\exp\left(-\lambda_1 (L_1 + L_2)\right)}{1 - \exp\left(-2\lambda_1 (L_1 + L_2)\right)}$$

$$C = A\exp(\lambda_1 L_1) + \frac{\sigma_1 - \sigma_2}{2}$$

$$D = B\exp(\lambda_2 L_1) + \frac{\sigma_1 - \sigma_2}{2}$$

3 Results and Discussions

A fully depleted n-channel Dual Material Gate Silicon on Insulator junctionless Transistor (DMG SOI JLT) simulated using COGENDA TCAD 2-D device simulator. DMG SOI JLT considered here is having uniform doping source, drain and channel region. Work function values of gate material-1 are 4.77eV and gate material-2 is 4.1eV respectively. DMG SOI JLT surface potential model verify with COGENDA TCAD 2-D device simulator [3].

Fig.2 shows the variation of channel potential along the channel with different drain voltage. Channel potential=surface potential-bulk potential. Analytical and observed simulated values of channel potential (channel po-

tential=surface potential-bulk potential) are plotted against horizontal distance χ in the channel for channel length of 40nm at different drain biases. It has been observed that due to the work function difference of gate M_1 and gate M_2, there is very less potential changes under gate M_1 when drain bias is increased. In a junction-less transistor current flows through the bulk and not through surface side. When drain voltage increase then bulk potential increases and overall channel potential decreases when V_{DS} is increased. After saturation, drain voltage (V_{DS}) has a very less influence on drain current and drain conductance is reduced [11].

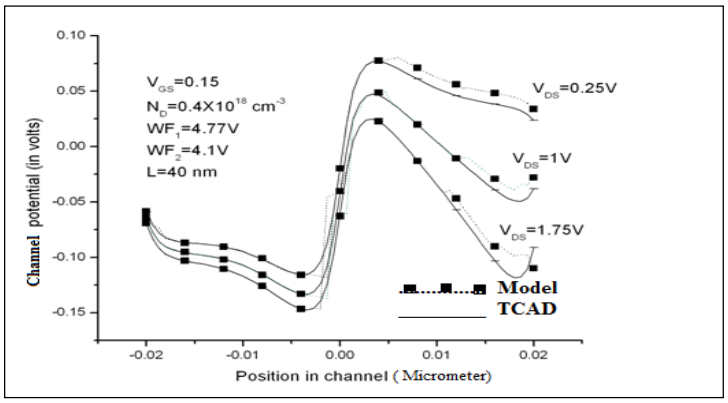

Fig.2 channel potential variation through channel at different drain voltages. The parameters used are t_{ox}=1nm,t_b=360nm,t_{si}=10nm and V_{sub}=0V.

At source side very less variation in bulk potential due to drain voltage variation.Fig.2 shows that DIBL effect is very less of DMG SOI JL MOSFET [12][13].Advantage of junctionless transistor is potential variation in bulk at source side is very less compare to surface side. Bulk Potential model very well correlate with the simulation result.

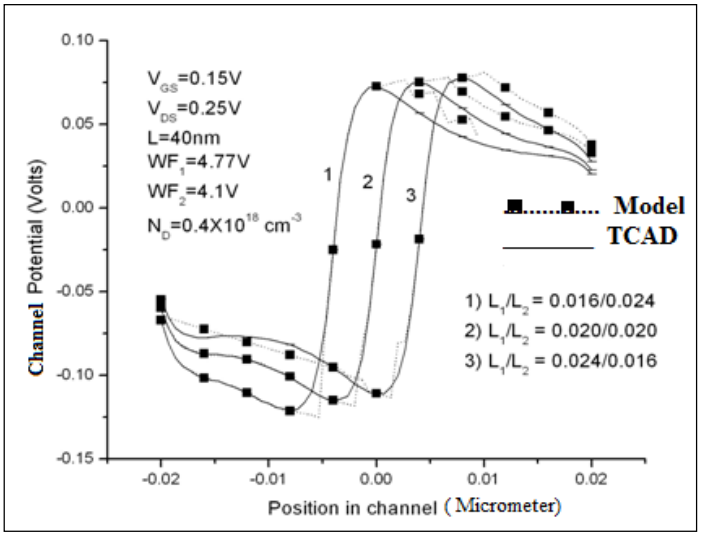

Fig.3 Variation of gate length L_1, L_2 and total channel length constant versus channel position along the channel.

Fig.3 shows that the changes of channel potential along the channel for different gate length L_1 and L_2 and total gate length remains constant. When L_1 is smaller than L_2 then peak of channel potential shift towards source side means peak electric field shift towards source side. Peak electric field shift towards source side then more electron accelerate from source side, hence current driving capability increases and hot electron effect problem reduces because peak potential shift towards source side [3]. When gate length L_2 smaller than L_1 then peak potential shift towards drain side.

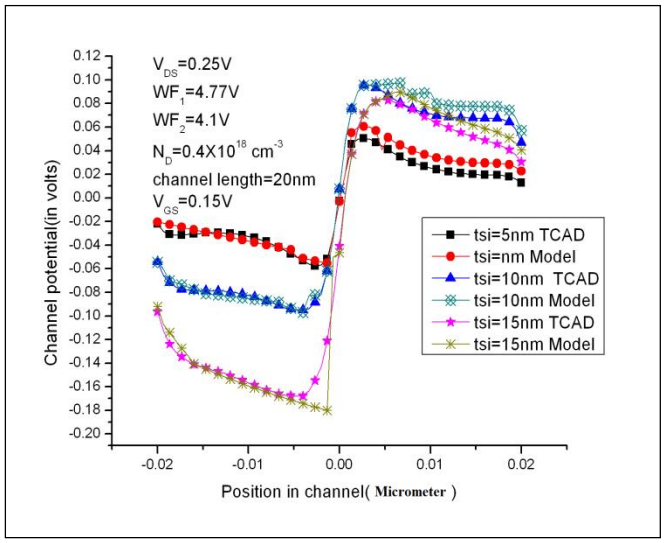

Fig.4 Channel potential variation along the channel obtained from the TCAD simulation a channel length L=40nm and drain bias V_{DS}=0.25V. The parameters used are V_{GS}=0.15V, t_{ox}=1nm, t_b=360nm,t_{si}=5,10, 15nm,V_{SUB}=0V, N_D=0.4x10^{18}cm^{-3}

Fig.4 shows that the variation of channel potential (surface potential-bulk potential). It is observed that when channel thickness is increased then bulk potential in the channel increases. When channel thickness increases then hot electron effect problem also reduces. In junction less transistor bulk impact ionization occurs and inversion Mode transistor surface impact ionization occurs. Drain voltage variation on surface impact ionization is maximum compare to bulk impact ionization; hence hot electron effect problem is less in junctionless Transistor.

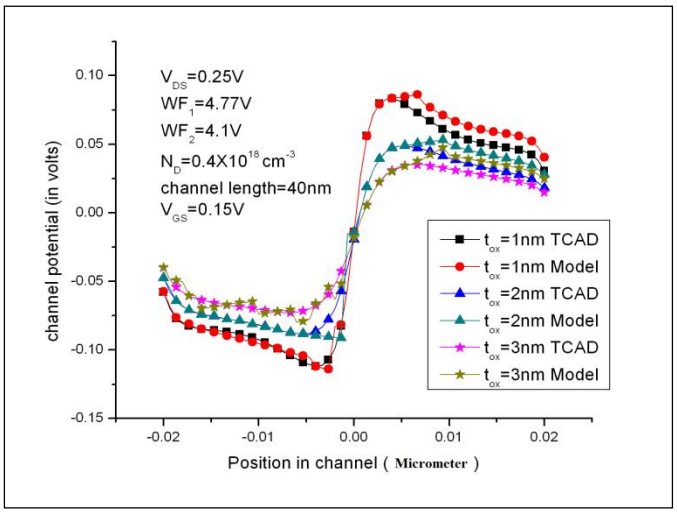

Fig.5 Channel potential along the channel obtained from the TCAD simulation a channel length L=40nm and drain bias V_{DS}=0.25V. The parameters used are V_{GS}=0.15V, t_{ox}=1nm,2nm, 3nm, t_b=360nm,t_{si}=10nm,V_{SUB}=0V, N_D=0.4X10^{18} cm^{-3} .

Fig.5 shows that the variation of potential in x-direcdtion at y=0 for t_{ox}=1nm,t_{ox}=2nm and t_{ox}=3nm. The drain voltage V_{DS}=0.25V and gate voltage V_{GS}=0.15V and remaining parameters are kept constant. Gate oxide thickness of DMG SOI JLT MOSFET increases then (surface potential-bulk potential) value increases meaning bulk potential decreases.In a junctionless transistor thickness of gate oxide increrases then DIBL effect is significantly reduces compare to less thickness of gate oxide.

4 Conclusion

The objective of this paper was to study analytical and simulated model of the DMG structure of junctionless silicon on insulator MOSFETs for developing 2-D analytical channel potential model to suppress SCEs to comparing results with COGENDA TCAD simulations. The result shows that drain voltage increase then bulk potential increases at drain side and small effect on source side means DIBL effect is very small. It has been observed that in dual material gate L_1 is smaller than L_2 then bulk potential shift towards source side and electron driving capability increases. Moreover, gate oxide thickness variation and gate length ratio affect on channel bulk potential and characteristics of the device.

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