Analysis of Various Adder Circuits for Low Power Consumption and Minimum Propagation Delay.

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Abstract. Arithmetic operations are important and most commonly used functions in VLSI applications. 1-single bit full adder digital circuit is the building block that performs the operations such of addition, subtraction, multiplication, etc. Designing, Implementation of single bit full adder circuits in nm submicron process and 45nm deep submicron process are evaluated in this paper. Three adder circuits considered are Conventional adder, Mirror adder and transmission gate logic adder are evaluated in this paper. Schematic and Layout of all three adder circuits in both micron process are administered with D.C and pulse inputs. Evaluation of power-delay product, parasitic capacitance and comparison between performance of adder circuits in both process are asserted. The adders are Modeled using EDA-Electric tool and LT spice simulation software.

Keywords: ***Adder, 45nm, D.C analysis, Power-delay-product, Electric tool.***

1 Introduction

Arithmetic operations are important and most commonly used functions in VLSI applications, digital signal processing, image processing etc. The full adder is typically the most critical element in digital circuit designs that rely upon arithmetic operations at their core, including digital signal processor (DSP), Microprocessor units and high speed encryption units. As the performance of the adder circuits has maximum on the overall system performance, Optimization of adder in terms of speed area and power dissipation remains an active area of research. With continued advances in processing technology, IC fabrication facilities now process has now designs at 35nm, 65nm, 45nm.

Modeling of full adder circuit at transistor level from Integrated Circuit point of view (Schematic, Layout) to achieve low power consumption and minimum propagation delay is an important factor [1]. The paper focuses on a approach for integrated Circuit design specification of the desired behavior of detailed physical design by EDA tools [4]. Electric tool is an Electronic Design Automation tool (EDA) used to design Schematic and Layout of full adder circuit and LT spice simulation carryout the circuit, process and logical simulation of designed circuits. The Full adder circuits under analysis are:-

1. Conventional adder model.
2. Mirror adder model.
3. Transmission gate logic adder model.

In this paper evaluation of adder circuits is executed using Predictive technology model at nm and 45nm technology node [11]. The power calculations, propagation delay, rise time, fall time calculations, propagation delay, area and perimeter occupied by individual transistor of above circuits, result and conclusion.

2 Single Bit Full Adder

A single bit full adder adds three one bit inputs numbers; A, B, and Cin to give sum and carry as outputs. A and B both are operands and Cin is a bit carried in from the previous less significant stage [6][8]. The full adder deals with an input carry bit resulting an improvement in accuracy and incorporation in cascading for multiple stage.

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The truth table of the full adder circuit clearly explains the consideration of Cin bit from the previous less significant stage for calculation of sum and carry of the next stage.

Table.1. Truth Table

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

2.1 Conventional adder

It is the basis of all single bit full adder design for future research, development and optimization. Logical modification of boolean equations ramifies into a single bit full adder with 28 transistors design. The model is represented in CMOS logic [7].The moderation is advantageous as there is a logic share between sum and carry subcircuits. The complement carry signal is used to generate the sum output. The following is an example of reorganized equation set for sum and carry:-

$$\text{Carry} = (A.\ B) + [\text{Cin}\ (A + B)] \qquad (1)$$

$$\text{Sum} = (A + B + \text{Cin}) + [(A + B + \text{Cin}).\overline{\text{Carry}} \qquad (2)$$

The sum and carry functions are represented by nested NMOS and PMOS transistors. The nested 14 series-parallel NMOs are connected between output and ground; the nested 14 series-parallel PMOS are connected between output and power supply. Two inverting circuits are required for re-inverting the sum and carry outputs. The circuit uses carry signal the generate sum hence the outputs are co-dependent. Using Electric tool and Lt spice simulator Schematic of Conventional adder model is shown in Fig-1

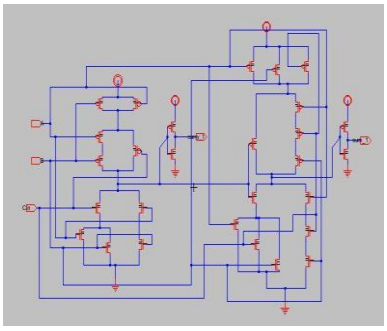

Fig.1. Schematic Conventional full adder circuit.

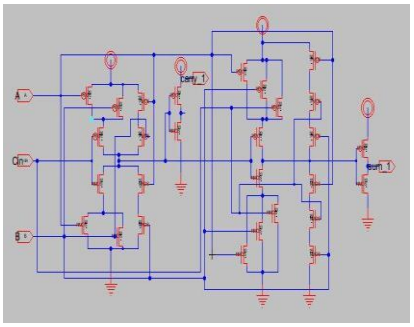

Fig.2. Schematic Mirror full adder circuit

2.2 Mirror adder

The Mirror adder the PMOS and NMOS networks are equivalent to each adder for both sum and carry outputs leading to fully symmetric circuit topology. The current in both PMOS and NMOS symmetric network is equal and mirror of each other hence Fully symmetric current mirror circuit. The functioning of Mirror adder is based on following parameters and Boolean equations:-

P-propagate; it propagates the carry generated in the previous stage.
D-delete; deletes the carry bit.

G-generate; generates the carry from inputs.

$$G = A.B$$
$$D = \overline{AB}$$
$$P = A\ XOR\ B$$

$$SUM = P\ XOR\ C_{in}$$
$$Carry = G + (P.C_{in})$$

Using Electric tool and Lt spice simulator Schematic Mirror adder model is shown in Fig-2. The PDN and PUN are logical implementation of propagate/generate/delete function. When either D or G is high, Co is set to V_{dd} or ground, respectively. When the condition for propagate are valid (P=1) the incoming carry is propagated (in inverted format) to Co. This results in considerable reduction in both area and delay. The NMOS and PMOS chain are symmetrical yielding correct operation. Sum and carry functions are follow self-duality resulting in a maximum of two series transistors in carry-generation[6].Because of the symmetry in PMOS and NMOS networks in both sum and carry network the transistor area covered in Mirror adder by PMOS network is less than that of conventional adder.

2.3 Transmission Gate Logic Adder

A full adder implemented based on transmission gate logic is a 20 transistor adder design. The technique builds on the complementary properties of NMOS and PMOS transistors. It uses the ideal approach and uses an NMOS to pull down and PMOS to pull up. It combines the best of both device flavors by placing an NMOS device in parallel with PMOS.

Complementary control signals are applied to the trans-mission gates which acts a bidirectional switch. When control signal=1 the NMOS and PMOS are both turned on and the input is passed. For charging output to Vdd: the input is set to Vdd the NMOS would charge up to Vdd-Vtn and turn off. Since the PMOS device is present and on the output charges all the way upto Vdd. Thus Transmission gate logic adders overcomes the problem of Pass transistor logic adders by enabling rail-to-rail swing of the output. TGL adder satisfies the following Boolean equations:-

X=A xor B
Sum=[bar(X) and Cin] or [X and bar(Cin)]
Carry=[bar(X) and Cin] or [A and bar(X)]

Using Electric tool and LT spice simulator Schematic TGL adder model is show in Fig 3 for TGL adder functioning is based on propagate generate model[6][7].The Xor of input A and B is used to select the true or complimentary valu of input carry as the new sum output. Based on the propagate signal the output carry is either set to input carry or either one input A or B.

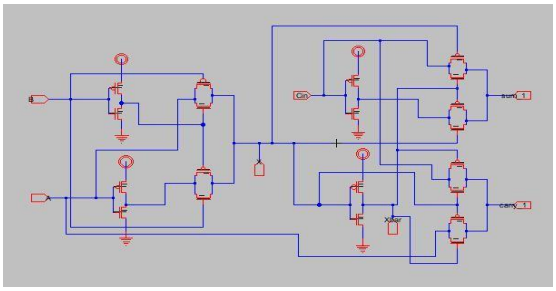

Fig. 3. Schematic TGL full adder circuit-Electric tool

3 Implementation of Adder Designs In 500nm Process

Electric tool is used to model the Schematics and Layouts of the adder designs and LT spice software is used to carry out the simulation.500nm- C-5 model file is used for evaluation and the transistor sizing for PMOS and NMOS considering the worst case delay.The 500nm C-5 model file used has process parameters specified Vdd=5V, Vthn=0.669V, Vthp=-0.669V, Tox=1.39e-008. In Electric tool the Lambda (scale) should be in the range of 250nm -300nm.The PMOS and NMOS actual length and width is decided by the multiplying factor of L,W of individual transistors of the set lambda.L=5 W=10 in Electric tool actual L=5*300nm=1.5um W=10*300nm=3um.The layout follows all MOSIS design rule specifications for mocmos. For the modeling of the three single bit full adder models the following transistor sizing are considered:-
For 500nm process the Lambda(scale for multiplication) is equal to 300nm(for mocmos) as per MOSIS design rule.

- Inverter ratio of NMOS is set $Z_n=(W/L)_n=2$.
- Inverter ratio of PMOS is set $Z_P=(W/L)_p=4$.
- Aspect ratio of PMOS and NMOS is set as $A= Z_n/ Z_P =2$. Length of all transistors is constant L=1.5um(L=5 in Electric scale)and W=3um(W=10 in Electric scale).

The LT spice simulation of schematic and layout gives the length and width of drain/sourse,area occupied by drain/source, perimeter of darin/souce. As/AD-area occupied by drain/source, PS/PD- perimeter covered by drain/source.

3.1 Conventional adder

The LT spice simulation of Conventional adder Layout Fig:-4 gives the following designed parameters of the adder:-

- Mnmos@0 gnd A-1nmos@0-poly-right net@1 gnd NMOS L=1.5U W=3U AS=3.75P +AD=5.165P PS=6.5U PD=7.567U
- Mpmos@0 vdd carrybar-8pmos@0-poly-left carry vdd PMOS L=1.5U W=6U AS=7.425P +AD=10.05P PS=12.3U PD=11.833U

3.2 Mirror adder

The LT spice simulation of Mirror adder Layout Fig:-5 gives the following designed parameters of the adder:-
Area and Perimeter covered by individual PMOS and NMOS drain and source of Mirror adder:-
Mnmos@6 net@5 A-1nmos@6-poly-right gnd gnd NMOS L=1.5U W=3U AS=5.612P +AD=3.15P PS=8.186U PD=5.1U
Mpmos@6 net@21 A-0pmos@6-poly-left vdd vdd PMOS L=1.5U W=6U AS=10.864P +AD=6.3P PS=12.814U PD=8.1U

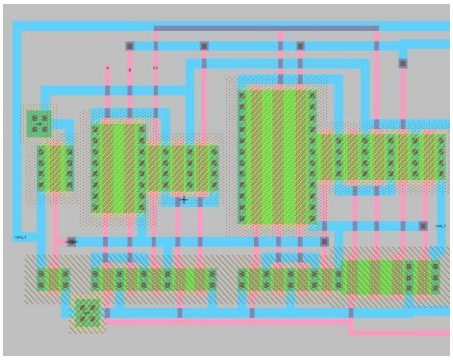

Fig. 4. Layout Conventional full adder circuit 500nm

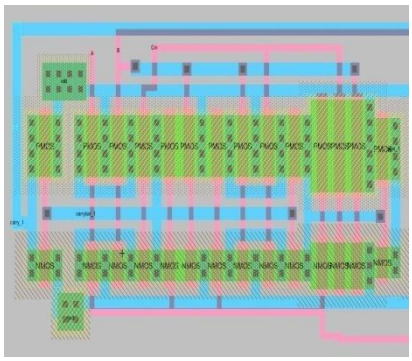

Fig.5. Layout Mirror full adder circuit 500nm

3.3 Transmission Gate Logic(TGL) Adder

The LT spice simulation of TGL adder Layout Fig:-6 gives the following designed parameters of the adder:-

Area and Perimeter covered by individual PMOS and NMOS drain and source of TGL adder:-

- Mnmos@9 net@193 X-32nmos@9-poly-left sum gnd NMOS L=1.5U W=3U AS=7.425P +AD=7.425P PS=12.3U PD=12.3U
- Mpmos@9 vdd Cin-17pmos@9-poly-left net@193 vdd PMOS L=1.5U W=6U AS=7.425P +AD=14.58P PS=12.3U PD=18.9U

Conventional adder has the highest total area covered and Mirror adder has the least TGL adder is wider amongst the three adders.

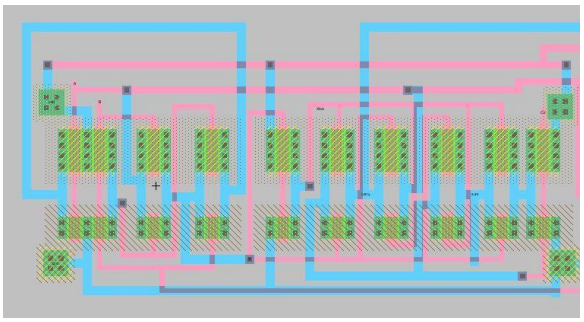

Fig. 6. Layout TGL full adder circuit 500nm

4 Implementation of Adder Designs in 45nm Process

In Electric tool the Lambda (scale) for multiplication should greater than half of the process technology i.e for 45nm should be in the range of 25nm -30nm.The PMOS and NMOS actual length and width is decided by the multi-plying factor of L,W of individual transistors of the set lambda. L=5 W=10 in Electric tool actual L=5*25nm=0.125um W=10*25nm=0.25um.The layout follows all MOSIS design rule specifications for mocmos.

For the modeling of the three single bit full adder models the following transistor sizing are considered:-

For 45nm process the Lambda(scale for multiplication) is equal to 25nm(for mocmos) as per MOSIS design rule.

- Inverter ratio of NMOS is set $Z_n=(W=L)_n=2$.
- Inverter ratio of PMOS is set $Z_P=(W=L)_p=4$.
- Aspect ratio of PMOS and NMOS is set as $A= Z_n/ Z_P =2$.
- Length of all transistors is constant L= 0.125um (L=5 in Electric scale) and W=0.25um (W=10 in Electric scale).

The LT spice simulation of schematic and layout gives the length and width of drain/sourse,area occupied by drain/source, perimeter of darin/souce.As/AD-area occupied by drain/source, PS/PD- perimeter covered by drain/source.

4.1 Conventional adder

The LT spice simulation of Conventional adder Layout Fig:-7 gives the following designed parameters of the adder:-

Area and Perimeter covered by individual PMOS and NMOS drain and source of Conventional adder:-

- Mnmos@1 gnd A-0nmos1-poly-left net@0 gnd nmos L=0.125U W=0.25U AS=0.026P +AD=0.035P PS=0.542U PD=0.625U

- Mpmos@4 vdd B-2pmos@4-poly-left net@34 vdd pmos L=0.125U W=0.5U AS=0.031P +AD=0.06P PS=0.625U PD=0.931U

4.2 Mirror adder

The LT spice simulation of Mirror adder Layout Fig:-8 gives the following designed parameters of the adder:- Area and Perimeter covered by individual PMOS and NMOS drain and source of Mirror adder:-

- Mnmos@0 gnd A-7nmos@0-poly-left net@0 gnd nmos L=0.125U W=0.25U AS=0.026P +AD=0.039P PS=0.542U PD=0.682U
- Mpmos@0 vdd A net@66 vdd pmos L=0.125U W=0.5U AS=0.052P AD=0.065P PS=0.875U +PD=1.004U

4.3 Transmission Gate Logic (TGL) Adder

The LT spice simulation of TGL adder Layout Fig:-8 gives the following designed parameters of the adder:- Area and Perimeter covered by individual PMOS and NMOS drain and source of TGL adder:-

- Mnmos@0 net@3 B-1nmos@0-poly-right gnd gnd nmos L=0.125U W=0.25U AS=0.073P +AD=0.052P PS=1.2U PD=1.025U
- Mpmos@0 net@3 B-0pmos@0-poly-left vdd vdd pmos L=0.125U W=0.5U AS=0.101P +AD=0.052P PS=1.575U PD=1.025U

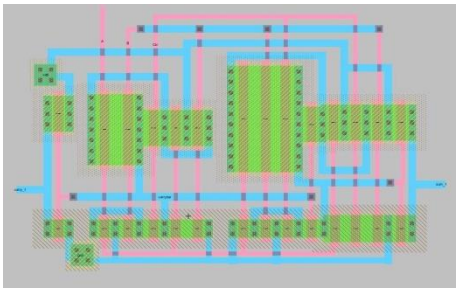

Fig.7. Layout Conventional full adder circuit 45nm

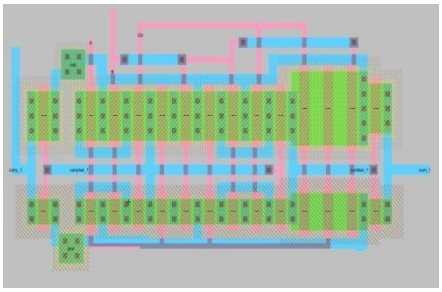

Fig. 8. Layout Mirror full adder circuit 45nm

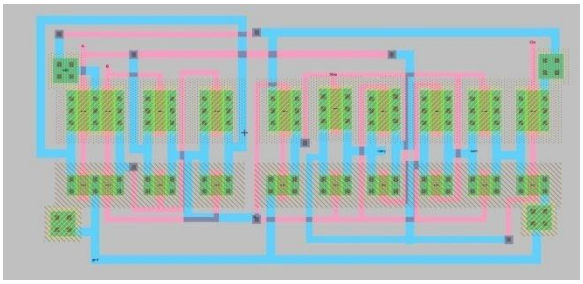

Fig. 9. Layout TGL full adder circuit 45nm-Electric tool.

5 DC Input Analysis and Simulation Results

DC Inputs are applied to Schematic and layout of the circuits. The Table 2 below depicts the static power consumed by all the three address in 500nm process. The Table 3 below depicts the static power consumption of the Conventional adder is highest followed by Mirror adder and Minimum by TGL adder in 45nm process. The high VDD=5V results in high static power consumed even though the Ivdd current is low.The high vdd is a drawback. The static power consumption of TGL adder is higher because in TGL all NMOS and PMOS transistors are on and the static power consumed is higher than conventional and mirror adder is not significantly large at different DC inputs. For 45nm process static power consumed is higher because of factors such as subthreshold current, DIBL, hot electron effect etc.

DC input ramifies that for different dc inputs the different amount of load current is consumed. Hence for each variation in input different no of transistors are switched on and consume variable power. Above observation can be used for an adder circuit when in ideal mode can be applied the D.C input that consumes the minimum power and hence desired results of power saving are achieved.

Table.2. Conventional, Mirror, TGL Adder Static Power Results 500nm

DC Inputs	CMOS(pWatt)	Mirror(pWatts)	TGL(pWatts)
000	224.35	224.35	400.09
001	244.35	244.35	300.07
010	150.03	223.5	400.09
011	150.03	187	300.075
100	261.81	187	300.02
101	263.34	243.6	200.05
110	261.81	243.6	300.01
111	241.95	223.6	200.05

Table.3. Conventional, Mirror, TGL Adder Static Power Results 45nm

DC Inputs	CMOS(nWatt)	Mirror(nWatts)	TGL(nWatts)
000	38.498	31.13	400.09
001	30.353	28.26	30.8
010	30.675	27.85	30.33
011	24.19	15.908	28.91
100	29.86	29.35	3.064
101	22.99	15.989	1.093
110	22.987	17.035	16.478
111	2.571	2.094	1.093

Pulse Input Analysis and Simulation Results.

Table.4. Adder Parameter-45nm

Adder parameters	Conventional	Mirror	TGL
Rise(ns)	0.5476	0.379	0.596
Fall(ns)	0.36	0.365	2.82
Delay(ns)	1.345	1.01	1.138
Pavg(uWatt)	1.51	1.125	0.556
PDP(e-015)	4.065	2.273	1.264
TotalArea(e-4) m^2	9.019	5.643	8.85

Table.5. Adder Parameter-500nm

Adder parameters	Conventional	Mirror	TGL
Rise(ns)	1.91	1.88	2.23
Fall(ns)	2.28	1.65	2.82
Delay(ns)	3.101	2.035	2.28
Pavg(uWatt)	712.1	456.67	243.23
PDP(e-012)	4.41	1.85	1.109
TotalArea(e-3) m^2	9.535	5.95	9.05

A Pulse simulation provides the total area, rise and fall time of output signals, propagation delay, power, power delay product of output signal. The load of the circuit is itself i.e output carry of 1st stage is connected to the input Cin of 2nd stage of the same circuit. The inputs are kept same for both the stages. Fig(9,10,11,12,13,14) shows the LTspice simulation output of all three adders respectively. Following are the pulse inputs applied to the adders:-

- vin1 A 0 dc 1
- vin2 B 0 pulse 0 1 0n 0n 0n 30n 60n
- vin3 Cin 0 pulse 0 1 8n 0n 30n 60n

The mirror adder has the lowest parasitic capacitance amongst the three followed by conventional adder and TGL adder. The effect of parasitic capacitances is highest on TGL adder due to which delay is increased slightly. Mirror adder has moderate propagation delay.The average power consumption is notified in table 4,5.The TGL has minimum average power consumption when compared to conventional and mirror adder ramifying in lowest power-delay-product.The conventional adder has the highest average power-delay product,high average power consumption resulting in highest P-D-P.
P-D-P of mirror adder is less conventional adder, mirror adder in 45nm and 500nm process and its respective TGL adder design in 500nm process. The power consumed by application of DC inputs in 45nm process is less than its respective model in 500nm process. The PDP of mirror adder is approximately equal to conventional adder in 45nm process and less than respective mirror adder design in 500nm process.

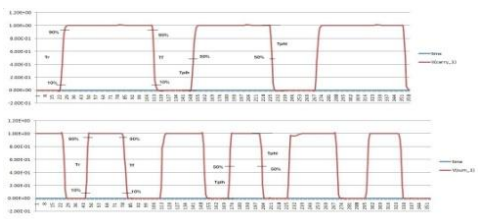

Fig.10. 45nm Pulse output-Conventional adder

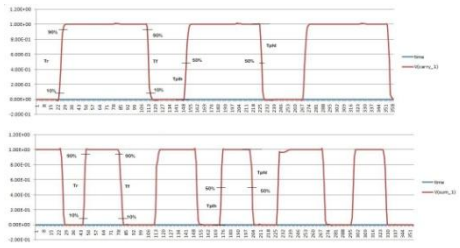

Fig.11. 45nm Pulse output-Mirror adder

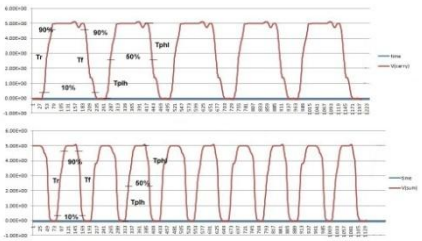

Fig. 12. 45nm Pulse output-TGL adder

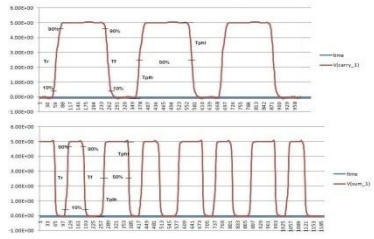

Fig.13. 500nm Pulse output-Conventional adder

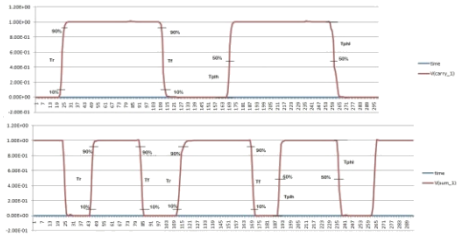

Fig.14. 500nm Pulse output-Mirror adder

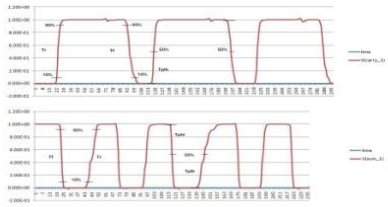

Fig.15. 500nm Pulse output-TGL adder

6 Conclusion

Study and analysis of the three adder designs in sub-micron (500nm) and deep sub-micron(45nm) process gives extensive results. For 500nm as well as 45nm overall Static power consumed by TGL adder is high as compared to Mirror and Conventional adder because both PMOS and transistors are ON at the same time.

For 500nm process the range of variation is moderate as compared to 45nm has high range of variation. Mirror adder has the lowest propagation delay followed by Conventional adder and TGL adder. Pavg of TGL adder is lowest followed by Mirror adder and Conventional adder has highest Pavg. Power delay product of TGL is lowest as compared to Mirror and Conventional adder. TGL has highest parasitic capacitance. Conventional adder has the highest total area covered and Mirror adder has the least. The Static power consumption of the adders in 45nm process in higher than that of 500nm due to factors such as sub-threshold conduction, DBIL, hot electron effect etc. The average power consumption, P-D-P of all the three adder designs is significantly reduced in 45nm process than 500nm process.

The adder designs in 45nm process out performs the adder designs in 500nm process in almost every aspect of design. TGL adder out performs than conventional and mirror adder in terms power dissipation, P-D-P, static power consumption in 45nm process and 500nm process.

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