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A Sampling Holder Using a Bootstrapped Switch

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***Abstract*-This paper describes the design of a sampling holder, Using a higher linearity bootstrapped switch, by using the bottom plate sampling to offset the effect of charge injection effect, By using the capacitance flip type structure to reduce power consumption, designing a high gain and high speed operational trans-conductance amplifier to improve gain and speed.**

Keywords-sampling holder; bootstrapped switches; operational Tran conductance amplifier; cascade

I. INTRODUCTION

Sample and hold circuit is composed of analog switch, storage element and a buffer amplifier. It is located in front of the analog to digital converter. Comparing with the post stage circuit, the input signal changes are much larger in the amplitude and frequency. So the linear sample and hold circuit level is high. In order to improve the linearity of the sample holder and meet the requirements of high precision, this paper describes the design of a sampling holder.

II. THE DESIGN OF BOOTSTRAPPED SWITCH

Poor linearity of ordinary switch is not suitable for large signal and high precision application. The bootstrapped switch is often used in the high precision analog-to-digital conversion. Figure 1 shows the circuit structure of the classical bootstrapped switch.

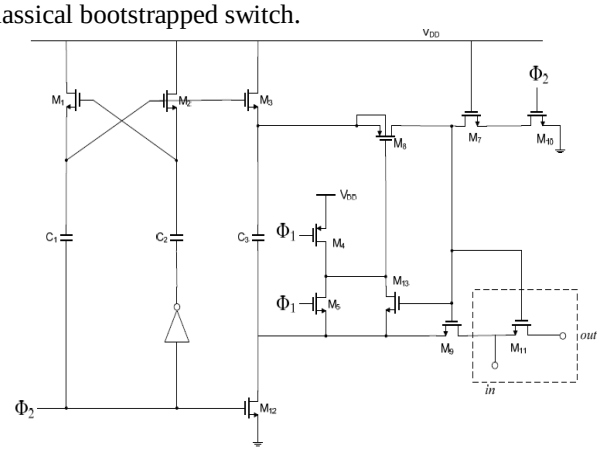

Figure 1. The structure of bootstrapped switch.

In figure1, the M11 is the core of the switch for the transmission of the input signal, all the rest are auxiliary switch. Φ 1 and Φ 2 is a two-phase non-overlapping clock. M3 and M12 and capacitor C3 form a charging circuit. They will charge C3 to voltage on VDD. This makes the gate -source voltage of M11 to maintain in this constant value at turn-on state. The role of the cross coupling M1, M2 and C1, C2 on the left is to constitute a voltage multiplier circuit, and improve s the voltage of the gate terminal of M3 to make C3 fully charged. The role of M8 and M9 is to partition and conducting the loop made by C3 in M11 pipe gate source end. The M4, M5 and M10 control them through. M7 and M13 according to the M10 and M8 play a protective role. The value of C3 must be large enough to avoid charge leaked M11 gate end parasitic capacitance.

Figure 2 shows the simulation results. The first line of the waveform is sine input signal and output signal. It can be seen that the output accurately track live input. Second waveform is the voltage differential between sampling switch gate terminal and the input terminal. The values in the conduction stage maintain a constant value to meet the purpose to increase the switch linearity.

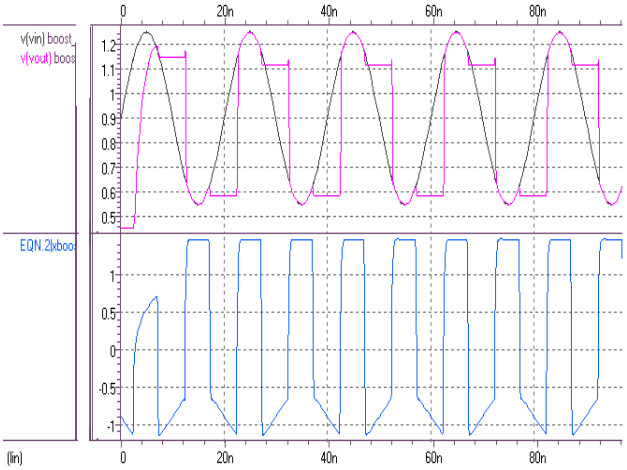

Figure 2. The bootstrapped switch waveform simulation.

III. THE SELECT OF THE SAMPLING CAPACITOR

The sampling capacitor is selected according to the requirement of noise and signal to noise ratio. The sampling holder noise is mainly composed of sampling phase switch thermal noise and keep stage operational amplifier thermal noise. By the derivation of estimation, we can the output equivalent noise of sampling holder.

$$P_{n,TH} = \sigma_{n,track}^2 + \sigma_{n,hold}^2 = 2\frac{1}{\beta}\frac{k_B T_r}{C_s} + 2\frac{4}{3}\frac{1}{\beta}\frac{k_B T_r}{C_{Leff}} \quad (1)$$

SNR of analog-to-digital converter is,

$$SNDR = \frac{P_{sig}}{P_q + P_n} = 74dB \tag{2}$$

In the formula, Psig is the signal power, and Pq is quantization noise power, and Pn is the total noise power. Setting up quantization noise power and total noise power are equal, it can estimate the size of the sampling capacitor.

IV. THE DESIGN OF OPERATIONAL AMPLIFIER

Operational amplifier is the key module in sampling holder. In order to realize the sampling holder with high speed and high precision, we need to design the operational amplifier with high DC gain, high bandwidth, and high swing. When designing, we should estimate operational amplifier index according to the sampling holder index to select the structure of the operational amplifier. Then we can choose parameters of each MOS according to the index value of amplifier, and adjust through simulation result. Because the circuit is fully differential structure, the design of the common mode feedback circuit is essential.

A. Determine the Dc Gain

Finite DC gain will produce static error. According to the static error allowed we can calculate the DC gain of the operational amplifier. With static error sampling holder for 1/4LSB, we can get ε_{static}

$$\varepsilon_{static} = \frac{1}{A \times \beta} < \frac{1}{4} LSB \tag{3}$$

Then we can get

$$A \times \beta > \frac{1}{\frac{1}{4} LSB} = 2^{N+2} \tag{4}$$

The N=12 substitution can be
$A \approx 84dB$

B. Determine the Unit Gain Bandwidth

The unity-gain bandwidth has something to do with Establish linear time and dynamic error. The total setup time consists of the establishment of large signal time and Establish linear time. It relates to the distribution of two stage setup time. We can estimate the proportion of the two establish time.

$$n = \frac{-\frac{C_{L,eff}}{\beta \times gm} \ln \varepsilon_{dynamic}}{\frac{V_{REF} - \sqrt{2} V_{ov}}{\frac{I_{tail}}{C_{L,eff}}}} \tag{5}$$

The corresponding values are substituted into Equation (5), then we can get n=4. The establishment of the total time is about half a clock cycle. Removing the non overlap time and clock edge, the effective establish time is about 4.6ns. So the linear establish time is 3.7ns, and slew time is 0.9ns. The loop unit gain bandwidth.

$$\beta \times GBW = \frac{1}{\tau} = \frac{-\ln \varepsilon_{dynamic}}{t_{linear}} \tag{6}$$

If

$$\varepsilon_{dynamic} = \frac{1}{4} LSB \tag{7}$$

Then

$$\beta \times GBW \approx 431MHz \tag{8}$$

At design time, GBW=600MHz.

C. Other Indicators

In order to establish the accuracy in a given time, we should also meet the requirements of the phase margin, in addition to meet the DC gain, gain bandwidth product outside unit. The phase margin has been explained in the front. In order to meet faster set goals, we Should make the phase margin at around 72 degrees. In addition, The operational amplifier should also meet the input differential swing and output one to the requirements of 1.5V in the power supply voltage of 1.8V.

According to the design index, we use a folded cascade gain bootstrap operational amplifier with the bigger input common mode range and high gain. Figure 3 shows the circuit diagram.

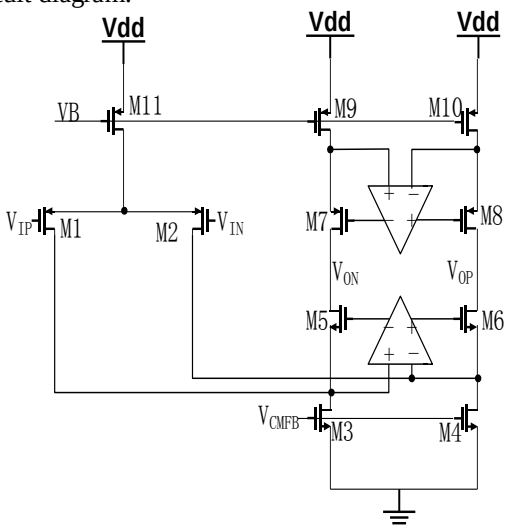

Figure 3. The folded cascade gain bootstrap operational amplifier.

V. THE SIMULATION OF OPERATIONAL AMPLIFIER

A. Design and Simulation of Main Operational

The main operational amplifier is the classic folded cascade structure, A PMOS tube is used as input, and witch has less 1/f noise. Using PMOS tube as input to the tube has another advantage is that substrate P transistor N that is well and the source end can be connected together amplifier. This structure can remove the back gate effect, and also has good symmetry. In addition, the current source in the folding point uses N tube to reduce parasitic capacitance. This design can achieve higher speed.

To the current circuit, in order to make the common source output branch common gate tube does not completely shut off, the output current should be slightly larger than the input current. In order to reduce the input parasitic capacitance, the input grid length should be for the minimum length of tube. In order to achieve higher gain, other transistor should take larger gate length. As current source, the MOS tube should take larger gate length to improve the accuracy of the current mirror and common mode rejection ratio. For input tube, should be properly decreasing the driving voltage in order to achieve greater efficient of transconductance. With low current gain greater transconductance, namely greater unity gain bandwidth product. In addition, the tube the input of the transconductance after also can inhibit the noise level. For the current pipe and common source common grid. Too much transconductance can introduce more noise, so we should take larger driving voltage. The larger driving voltage can make the matching degree of the current source pipe to be better. But the larger driving voltage will decrease voltage swing.

According to the above design idea, we designed the main operational amplifier. Small signal analysis of the operation amplifier, amplitude frequency and phase frequency response waveform, as show in figure 4. For two curves in a diagram the amplitude frequency and phase frequency response waveform. We can see by the simulation results of main operational unit gain bandwidth is 805MHz, and the DC gain is 52.7 dB, and the phase margin is 78 °.

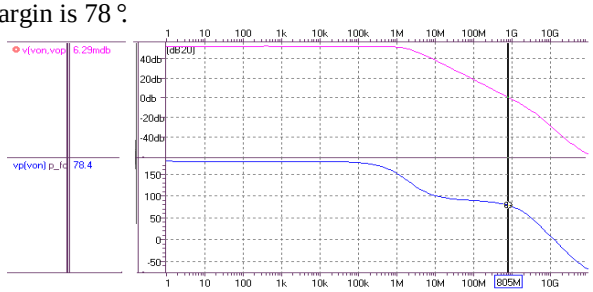

Figure 4. The main op-amp frequency characteristic

B. Design of Auxiliary Operational Amplifier

The too low gain of op-amp can not satisfy the static error, so we use auxiliary op-amp gain. Auxiliary op-amp adopts fold same source grid structure, and according to input level of discretion to choose the type of input on the tube. In the fold point potential is low, so choose P type tube. Similarly, another should choose N type tube.

Auxiliary op-amp access form the local loop, so the circuit design to consider stability. The common source common grid capacitance constitutes the load capacitance of auxiliary op-amp. When circuit design should ensure that the phase margin of auxiliary operational amplifier is large enough. The access of auxiliary operational amplifier also introduces a zero-pole extremely, located in the auxiliary op-amp unit gain bandwidth. A zero-pole is in the step response corresponding index of items. If the pole zero smaller, can slow down the whole movement of the step response. Therefore,the design should be the design of large enough. At the same time, we also should not be more than the main operational time poles caused by stability problems. The result can be expressed as the following formula.

$$\beta \times \omega_{u,main} < \omega_{u,boost} < \omega_{p2,main} \tag{9}$$

In the formula, ωu, main is the unit gain bandwidth of primary op-amp , and ωu,boost is the unit gain bandwidth of auxiliary op-amp , and is the second pole of primary op-amp, and β is the feedback coefficient.

C. The Overall Operational Simulation

Through auxiliary op-amp and the op-amp whole simulation, the amplitude frequency and phase frequency response waveform can be obtained. The waveform is shown in figure 5. Figure in the upper and lower express amplitude frequency and phase frequency response curve waveform respectively. By the simulation results can be seen that the op-amp unit gain bandwidth is 979MHz, and the current gain is 100dB, and the phase margin is 71.6 °. Through the analysis, we can know that the gain of the op-amp is main and the superposition of auxiliary op-amp. The increasing of the unit gain bandwidth is due to the folding point introduction of negative feedback, leading to the lower impedance, so the second pole is pushed to the further afield.

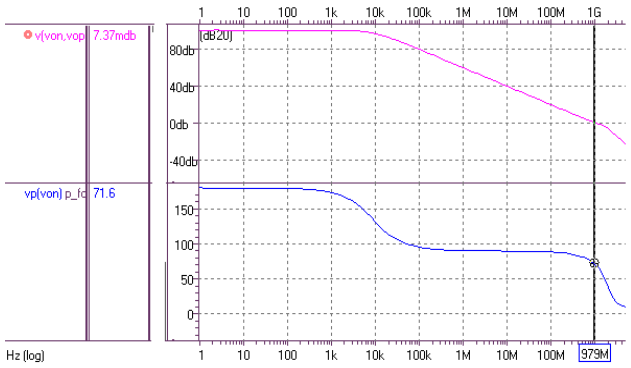

Figure 5. The overall op-amp frequency characteristic

D. The Loop Simulation

The op-amp is applied to closed loop circuit. In order to ensure the stability of the closed loop circuit, it is necessary in the loop simulation.

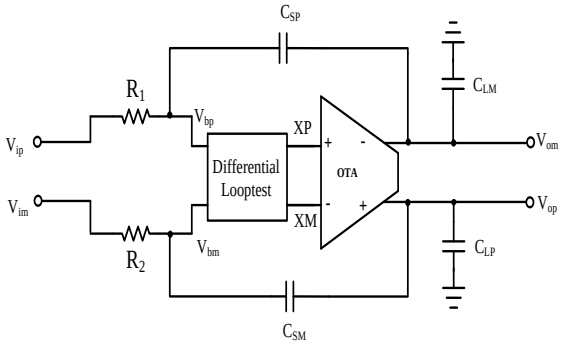

Figure 6. The simulation circuit of loop circuit of sampling keeping circuit

The simulation circuit is shown in figure 6, and the simulation analysis is based on a Middle Brook loop analysis method. The loop frequency characteristic simulation result is shown in figure 7.The resistance in the graph is to offer in the simulation to the op-amp common-mode input level.

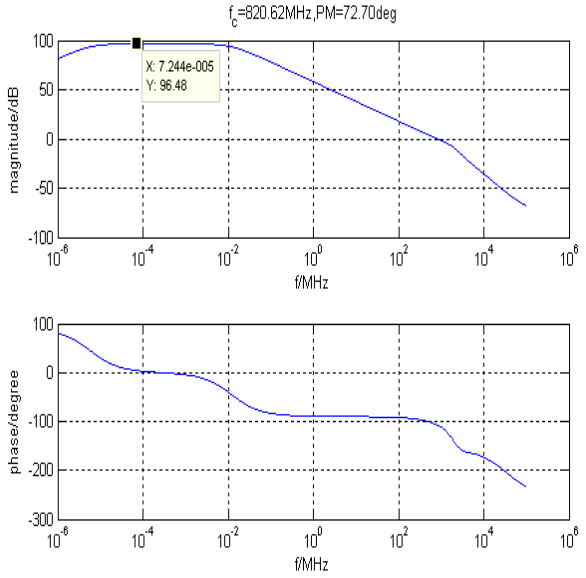

Figure 7. The loop frequency characteristic simulation result

E. The Simulation of Output Swing

When the output signal amplitude increases, the operational amplifier gain is reduced. In order to verify the design of output swing gain is large enough, we need the simulation was carried out on the operational amplifier output swing. The simulation result is shown in figure8. Through the simulation result, we can see that the amplifier gain is greater than 97.7dB, when the output swing is between -750mV and 750mV. The results meet the requirement of static error.

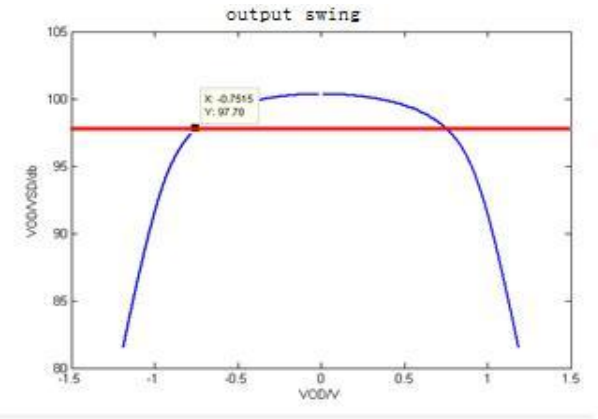

Figure 8. The output swing simulation result

F. The Common-Mode Feedback Circuit Design

Compared with the single side structure, fully differential structure has larger output swing and ability to resist noise and common mode rejection ratio. However the difference structure of the op-amp offset can not achieve self-sufficiency, and its output current depends on the two current source located in circuit above and below. When the current provided by above two current source is not completely equal, the output voltage will be significantly deviate from the set of common mode level. In order to solve this problem, we must use the common-mode feedback circuit to dynamically measure the common-mode output level. To the one of the current source to do corresponding adjustment, so as to stabilize the main output common-mode level. One Switched capacitor common mode feedback circuit is shown in figure9.

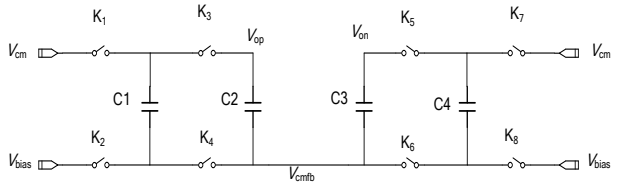

Figure 9. Switched capacitor common mode feedback circuit

The following briefly describes its working principle. The role of the capacitance C1,C4 is continuously update voltage difference on both ends, then recharge the capacitor C2,C3. As shown in figure 10, in the case that the charge is updated at the ends of the capacitor voltage V1,then V1=Vcm-Vbias. So we can get,

$$V_{cmfb} = V_{op} - (V_{cm} - V_{bias}) \tag{10}$$

$$V_{cmfb} = V_{on} - (V_{cm} - V_{bias}) \tag{11}$$

Two formula combined divided by two is

$$\frac{V_{op}+V_{on}}{2}=V_{cm}+(V_{cmfb}-V_{bias}) \tag{12}$$

As seen in formula(12), if Vcmfb and Vbias is equal, the output common-mode level is equal to Vcm.

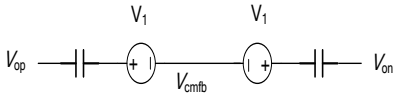

Figure 10. The equivalent circuit of switched capacitor common mode feedback circuit

G. The Sample Holder Dynamic Performance Simulation

Taking transient analysis to the sample holder, and taking fast Fourier transform to sample point, we can obtain dynamic characteristics of the sample holder. In the simulation, in order to avoid the spectrum leakage and same sampling point in one cycle, the relation between input signal frequency and sampling signal frequency should meet the follow formula.

$$\frac{f_{in}}{f_{clk}}=\frac{M}{N} \tag{13}$$

In the formula, fiin and fclk are the input signal frequency and sampling signal frequency respectively, and N is the number of sampling points, and M is the signal cycle number. N and M are integers, and they are prime Numbers.

Let the input signal frequency is 49.21875MHz, and peak to peak voltage is Vpp 1.5V, then we can get fast Fourier transform result of sampling point as shown in figure 11.

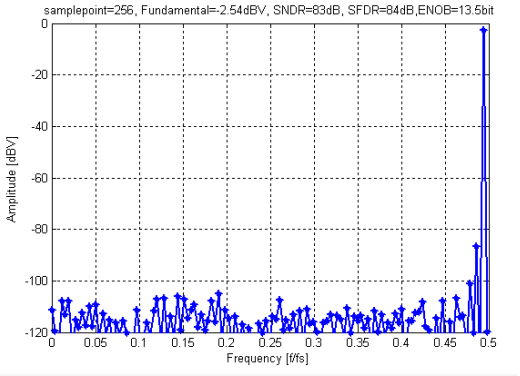

Figure 11. Dynamic characteristics of sample holder

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