

Design of a Full-Coherent Millimeter Wave Radar Frequency Synthesizer

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Abstract—In this paper, with the combination of DDS, PLL, multiplier and mixing techniques, a millimeter wave (mm-wave) full-coherent frequency synthesizer with low phase-noise and spurs is developed. It includes a mm-wave source. A linear frequency modulation (LFM) generator and a microwave source serving as the second local oscillator for the receiver. An external 100 MHz temperature-controlled crystal oscillator is used as the coherent clock for all the sources. The phase noise and spurs of the mm-wave signal have been analyzed and estimated. Measured results show that the output frequency is 34.855~34.865 GHz, the stepping frequency is 100 KHz, the output power is larger than 16 dBm, and the phase noise level is about -92 dBc/Hz at an offset of 10 KHz.

Keywords—*Millimeter Wave; Phase-Locked Loop (PLL); Direct Digital Synthesis (DDS); Frequency Synthesizer; Phase Noise*

I. INTRODUCTION

Millimeter wave (mm-wave) frequency synthesizer is one of the critical modules in modern mm-wave communication and radar systems. In order to achieve high resolution for small targets, the linear frequency modulation (LFM) sweep signals are widely employed in various pulsed

radars. There are several methods for frequency synthesizer design, including the direct digital synthesis (DDS), the indirect synthesis based on a phase-locked loop (PLL), frequency multiplier chains, and so on [1, 2]. The DDS can produce linear and agile frequency chirps, which are well suited for FM radar applications. Nevertheless, due to its limited usable clock frequency, it is not impossible to gain the desired mm-wave radar signals directly. Frequency multiplication techniques could translate RF signals into mm-wave signals. But the multiplier chains will degrade the phase noise and the spurs as the increase of multiplication times [3, 4].

In this paper, a frequency synthesizer for full-coherent mm-wave radar applications is presented. Combination of DDS, PLL and mixer techniques is employed to obtain attractive features of low phase noise, small frequency step sizes and low spur levels. Also, the overall architecture of the frequency synthesizer and the phase noise model of PLLs have been presented.

II. CONFIGURATION OF THE FREQUENCY SYNTHESIZER

The block diagram of the mm-wave frequency synthesizer is shown in Figure1.

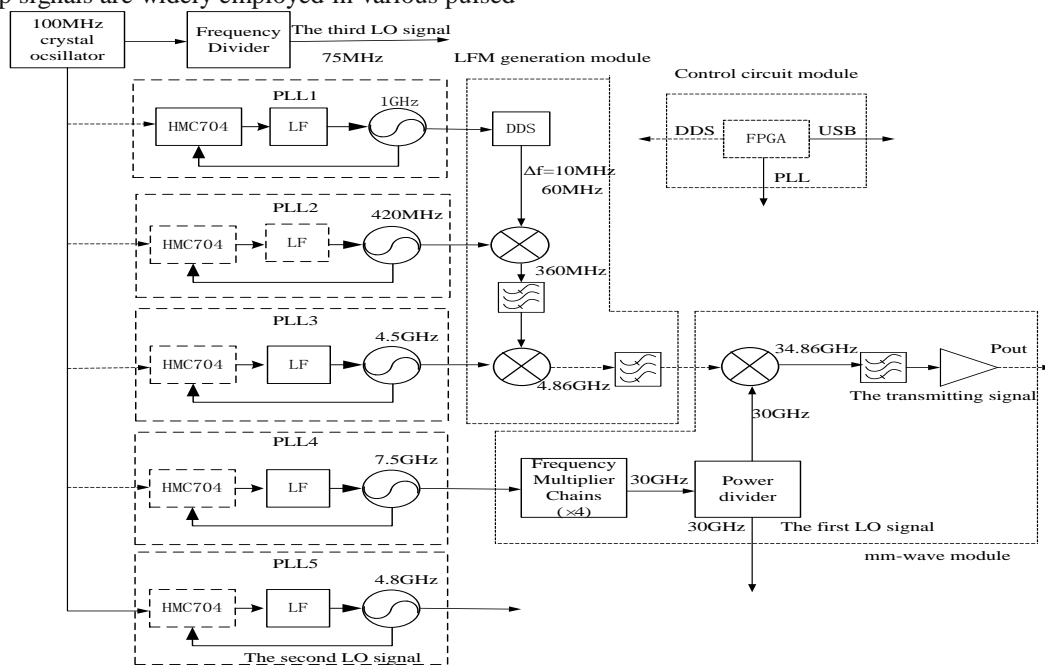


Figure 1. Block diagram of the mm-wave frequency synthesizer.

It consists of eight modules, and they are five phase-locked loops (PLLs), a LFM generation module, a mm-wave module, and a control circuit module. The frequency synthesizer provides four coherent output signals: the transmitting mm-wave LFM signal, the single frequency point mm-wave signal as the 1st local oscillator (LO), output signal of 4.8 GHz as the 2nd LO, and the 3rd LO for the digital intermediate frequency (IF) receiver. In addition, the external 100 MHz temperature-controlled crystal oscillator with a phase noise of -140 dBc/Hz at 10 KHz offset, is used as the reference signal. Meanwhile, the FPGA is adopted to control the DDS and the all PLLs.

For the DDS system, Analog Device's AD9910, has been used which has a feature of a 14-bit DAC operating up to 1 GSPS. The PLL1 module is designed to produce a 1-GHz signal as the sampling clock for the DDS chip. In this method, this is not only to minimize the output level of the spurious signals from the DDS output, but also increase the frequency resolution [5].

In the LFM generation module, the DDS outputs the LFM signal of 55~65 MHz, which has the stepping frequency of 100 KHz, and then mixed with the signal of 420 MHz, which come from the PLL2, to gain the 360 MHz signal with 10 MHz bandwidth. At the same time, through an up-converter bumping by 4.5 GHz signal, which comes from the PLL3, the 360MHz LFM signal is up-converted to 4.86-GHz as an input signal of the followed mm-wave mixer.

The mm-wave module has two functions, one is to generate a fixed 30-GHz signal as the first LO for the receiver, and another is to provide a LFM 34.86-GHz transmitting signal. To meet the practical requirements of the module, an up-converter and a low insertion loss mm-wave two-way power divider are used in the design. A 7.5-GHz signal from the PLL4 output is multiplied by 4 to obtain the 30 GHz continuous wave signal, which is to act as the input signal of the 2 way power-divider. An LFM mm-wave transmitting signal with lower phase noise is obtained by mixing the 4.86-GHz signal with the 30-GHz signal. In order to remove the spurious and undesired frequency components, a band pass filter (BPF) with narrow bandwidth is necessary to design carefully.

The HMC704 phase detector (PD) is used in this system, which can provide the tuning voltage to the maximum of +5.2 V. Except for the PLL5, the tuning voltage of all voltage-controlled oscillators (VCOs) is below +5 V, the passive loop filters (LFs) are enough to meet the practical requirements. Because the maximum PLL charge pump voltage of +5.2 V is lower than the 7.5 GHz VCO tuning voltage, an active third order loopfilter is adopted in PLL4. Considering phase noise and locking times, the phase detector (PD) frequency, loop bandwidth and phase margin are 50-MHz, 200-KHz and 60°, respectively.

III. PHASE NOISE ANALYSIS AND ESTIMATE

A. Phase Noise Estimate

In this module, though the frequency synthesizer is constructed by more complicated mixers, multiplier chains

and divider circuits, the phase noise of output signal can be estimated by using a simplified frequency synthesizer architecture, which can be used in mm-wave terminals. Figure2 shows the simplified block diagram of the mm-wave frequency synthesizer.

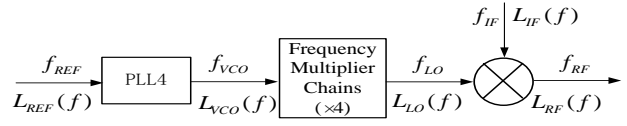


Figure 2. Signal model of the simplified millimeter-wave frequency synthesizer.

Here, f_{REF} , f_{VCO} , f_{LO} , f_{IF} and f_{RF} are the frequency of the reference crystal oscillator, the locked VCO in PLL4, the multiplier chains output signal, the LFM signal into the mixer, and the mm-wave output signal, respectively. Correspondingly, $L_{REF}(f)$, $L_{VCO}(f)$, $L_{LO}(f)$, $L_{IF}(f)$ and $L_{RF}(f)$ represent their phase noises. Generally, the output phase noise of a PLL frequency synthesizer is mainly determined by the VCO phase noise and the phase noise of the reference signal source [6, 7]. Because the $L_{VCO}(f)$ is much higher than the $L_{REF}(f)$, so the latter to the total phase noise contribution of the PLL4 can be neglected.

According to the datasheet of HMC704L, the PLL noise floor and the flicker noise can be computed using (1) and (2) (from [8]) as follows:

$$PN_{floor} = F_{p0_dB} + 10\lg(f_{pd}) + 20\lg(f_{VCO}/f_{pd}) \quad (1)$$

$$PN_{flick} = F_{p1_dB} + 20\lg(f_{VCO}) - 10\lg(f_{offset}) \quad (2)$$

Where $F_{p0_dB} = -233$ dBc/Hz and $F_{p1_dB} = -266$ dBc/Hz represent the figure of merit (FOM) for the phase noise floor and the flicker noise region, respectively. When the VCO locking at 7.5 GHz, we can get

$$PN_{floor} = -233 + 10\lg(50 \times 10^6) + 20\lg((7.5 \times 10^9)/(50 \times 10^6)) = -112.5 \text{ dBc/Hz@10 KHz} \quad (3)$$

and

$$PN_{flick} = -266 + 20\lg(7.5 \times 10^9) - 10\lg(10 \times 10^3) = -108.5 \text{ dBc/Hz@10 KHz} \quad (4)$$

Thus, the total phase noise of the PLL can be estimated as

$$L_{LO}(f) = 10\lg(10^{(PN_{floor}/10)} + 10^{(PN_{flick}/10)}) \approx -108.5 \text{ dBc/Hz@10 KHz} \quad (5)$$

Because the multiplier chains will increase the phase noise as N^2 , where N is the multiplication times [4], the $L_{LO}(f)$ can be given as

$$L_{LO}(f) = L_{VCO}(f) + 20\lg N \quad (6)$$

Here $N=4$, we can obtain $L_{LO}(f)=-108.5+20\lg 4\approx-96.5$ dBc/Hz @10 KHz. According to the analysis [9], the $L_{IF}(f)$ is far below than the $L_{LO}(f)$, so $L_{IF}(f)$ can be ignored. Thus, the $L_{RF}(f)$ is equals to the $L_{LO}(f)$ approximately.

B. Spurious Analysis

Because the spurs of the DDS are much higher than that of the PLLs, so the spurs of the system will be dominated by the DDS. In order to suppress the spurious components, the frequency tuning word (FTW) can be changed to obtain the lower spur levels. This is the key to restrict the spurious signal in the frequency synthesizer. Since the spur levels of the AD9910 chip are less than -86 dBc at the bandwidth of 500 KHz. Thus, its final output signal can meet the practical requirement that the spur levels are lower than -65 dBc.

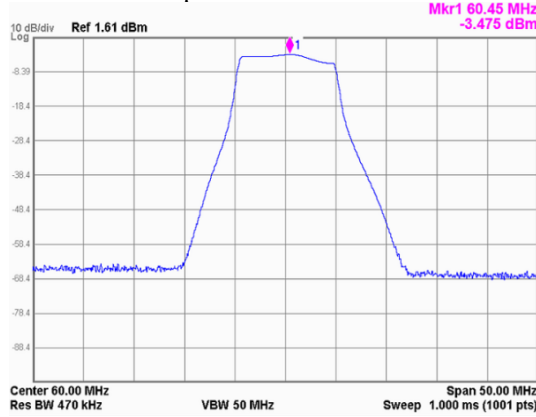
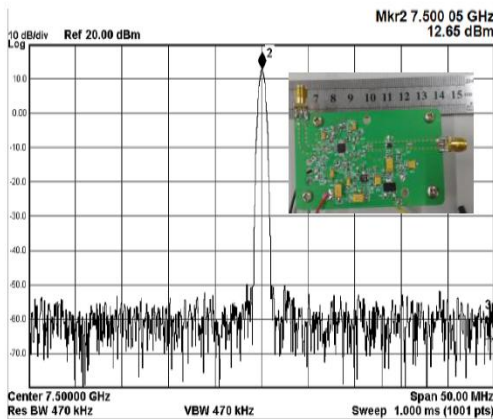


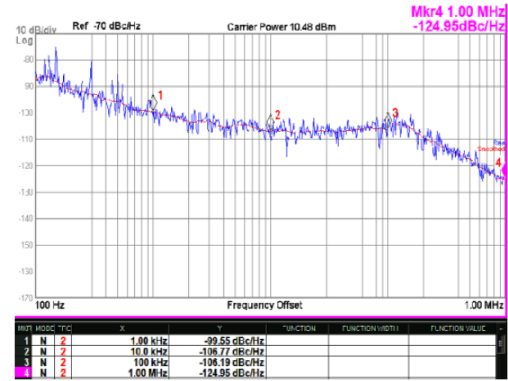
Figure 3. Measured spectrum of the DDS output at 60 MHz.

IV. EXPERIMENT RESULTS

In the frequency synthesizer, all the modules are fabricated and measured. The measured spectra of the DDS output at the center frequency of 60 MHz are given in Figure 3. The spur levels of the LFM signal are less than -65 dBc with the span of 50-MHz. The measured results agree well with the analysis ones. For the f_{LO} , the measured output power and phase noise spectrum are shown in Figure 4(a) and 4(b), respectively. From the spectra of f_{LO} in Figure4, the output power is about 12.6 dBm at 7.5 GHz, and $L_{VCO}(f)$ is -106.77 dBc/Hz at 10-kHz offset.

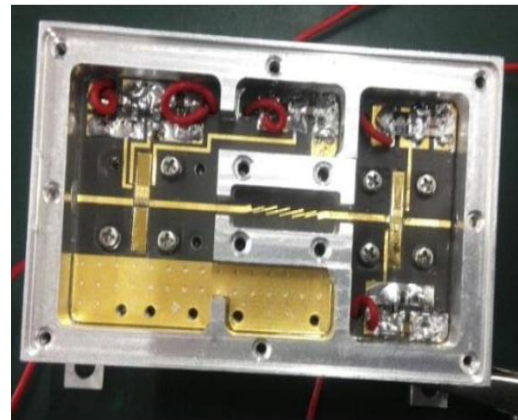


(a) Fabricated circuit and output power

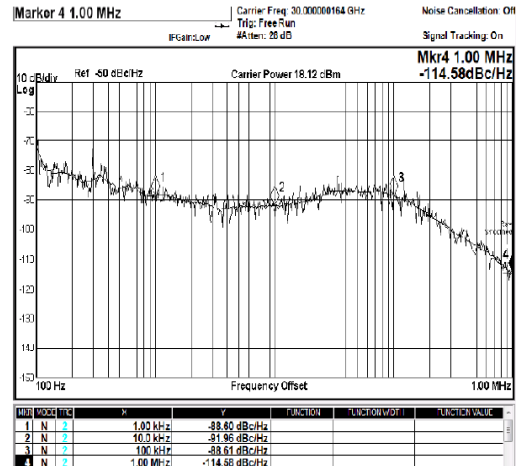


(b) Phase noise

Figure 4. Measured spectrum at 7.5 GHz



(a) Fabricated module



(b) Measured phase noise at 30 GHz

Figure 5. Photograph of the measured device

All measured and computed results show a good agreement, differing by no more than 1.7 dB at the range of 1-10 KHz offset frequency. The fabricated mm-wave multiplier module is shown in Figure 5(a). To confirm the method of phase-noise estimate for the multiplier chains, measured $L_{LO}(f)$ are also illustrated in Figure 5(b). The

measured phase noise is about -92 dBc/Hz at 10-kHz offset. In comparing to the estimated values, the test results are deteriorated about 4.5 dB at the same offset frequency. The main causes are the tolerance of the PCB fabrication.

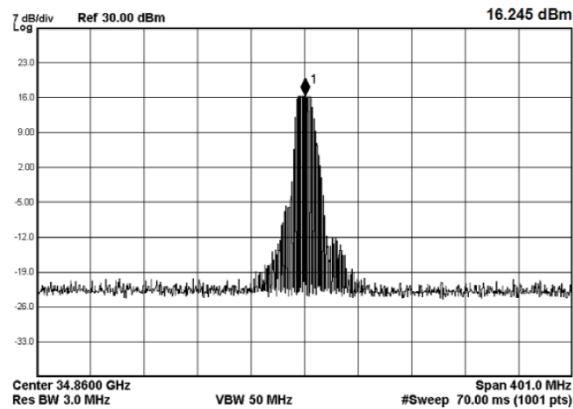


Figure 6. Measured output spectra of the mm-wave.

Figure 6 shows the spectra of the LFM 34.86 GHz transmitting signal. The measured output power is larger than 16 dBm, the sweep frequency range is 34.855~34.865 GHz, the stepping frequency is 100 KHz, and the spurious output is less than -40 dBc approximately. It is impossible to measure the phase noise of the LFM signal directly. However, according to the above analysis, we can estimate that the practical LRF(f) is about -92 dBc/Hz at 10 kHz offset. All the above results are tested by using Agilent signal analyzer N9030A. Figure 7 illustrates the photograph of the experimental device.

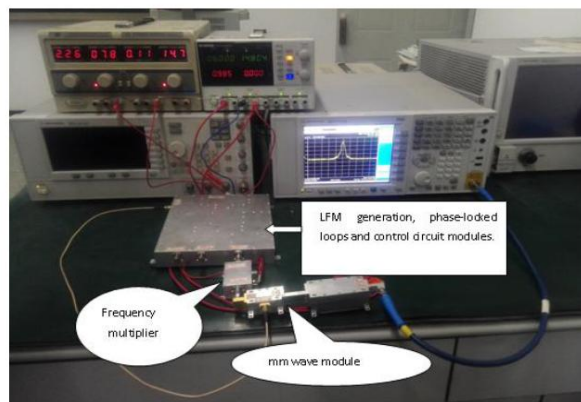


Figure 7. Photograph of the measured device.

V. CONCLUSION

In this paper, a full-coherent radar frequency synthesizer has been designed and implemented using combination techniques of multiplication, PLL, DDS and mixers. A simplified signal model is given to estimate the phase noise of the frequency. Measurement results demonstrate that the mm-wave frequency source achieves a frequency range from 34.855~34.865 GHz with a phase noise lower than -92 dBc/Hz at a frequency offset of 10 KHz.

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