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Channel Length, Drift-region Distance, and Unit-Finger Width Impacts on the HBM Robustness for the 600 V N-Channel LDMOS Transistors

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ABSTRACT: An UHV n-channel LDMOS transistor is usually used for the power management AC-DC convertor that need to enhance the ESD robustness to resist external transient noises. In the cost saving consideration, an UHV nLDMOS unit should be both acted as a circuit element and anti-ESD device because of its large layout area. In this work, modulations of channel length, drift-region distance, and unit-finger width of a single-finger and double-fingers 600 V UHV nLDMOS devices are focused to find out the apposite layout parameters trend. First, as for the single-finger device-under-test (DUT) samples, channel-length modulations devices were at least passed HBM 3.5 kV level under the reverse voltage polarity, and its HBM robustness passed 8 kV under the reverse voltage polarity. Next, the drift-region modulated devices can be at least passed HBM 6.75 kV level under the PS mode. In the NS mode zapping, its HBM robustness will be over 8 kV. On the other hand, as for the double-finger DUTs, experimental data were shown that the HBM ESD robustness is enhanced with increased width of DCG and channel width at least passed HBM 2.75 kV under the PS mode. All experimental devices can pass 8 kV anti-HBM ESD robustness for reverse voltage polarity.

1. INTRODUCTION

An Ultra-High-Voltage (UHV) process is a common integrated circuit fabrication technology of the power manage AC-DC convertor [1]-[4]. And, this power manage circuit has low-voltage (LV) CMOS control circuits, HV CMOS driver circuits, high-precision analog circuits and UHV lateral-diffused metal-oxide-semiconductor (LDMOS) power transistors. To compare with a traditional chips module, an AC-DC single chip [5]-[7] fabricated by an UHV Biplar-CMOS-DMOS (BCD) process technology has advantages like lower standby power consumption, high convert efficiency, low cost, and high reliability. However, these UHV LDMOS transistors are subject to high voltage sustainability and reliability requirement [8]-[10]. The reliability under electrostatic charge is special critical for power-managed ICs [11]-[12]. Therefore, it is also important that an UHV LDMOS power transistor can discharge huge ESD current efficiently or not. On the other hand, the layout issue has a big difference between UHV, low-voltage and medium-voltage applications, when a device which can sustain the UHV situation. Eventually, the relationship of fabrication size and protection unit has to considerate clearly. Unfortunately, seldom papers touch the ESD reliability due to these applications in a single chip is just starting up. Therefore, the ESD immunity of an UHV LDMOS study will be suffered an obvious challenge at this moment.

In this paper, 600V UHV N-channel LDMOS transistors (& gate-to-ground configuration) will be used. It is expected to have to sustain high electronic field, so that it has a long HV N-Well region in the drain-side. By added a low concentration layer (HV N-Well) and floating field-plate of poly-2 in the drain-side, the depletion region decreased the surface field and increased the breakdown voltage. Normally, the operating voltage of these UHV devices is operated at the 600 V condition, so that the size of them are larger than that of the middle-voltage LDMOS. For ESD protections, these testing samples are gate-grounded to form GGnMOS circuit architecture. To avoid making high electric field and high current on the device sharp edges, it is usually designed as a circular arc and the channel-width also enlarged enough in

layout. In this study, the channel-length, the drift region (DCG), and unit-finger width (W_f) modulating effects will be evaluated by a human-body-model (HBM) tester.

2. UHV NLDMOS DEVICES DETAILES

2.1 Single-finger UHV Cells

Cross-section view and schematic layout of an UHV nLDMOS device are shown in Figs. 1 and 2, respectively. In order to make a device can be sustained ultra high voltages, the drift-region distance was designed wide enough, the poly2 was added on top of the field-oxide layer and a long HV NWell region was built in the drain-side to increase the breakdown voltage of a device. These testing samples were fabricated by a TSMC T50UHV BCD process. Device parameters of the benchmark sample are as following: the channel length was 3 μm, the channel width was 300 μm, the DCG width (or called the drift-region distance) was 57 μm, and the finger number was 1.

Next, the channel length (L) of UHV LDMOS was to alter. By definition, the channel length is a distance between the HV N-well and source side. When the channel length is increased, then the channel resistance is increased and the passing current density per unit width will be decreased too. Obviously, a device can be survived due to a low current density. Nevertheless, some shorter channel lengths for comparison will be used in this sample group. Therefore, parameters of channel length (Group-1) were 0.9, 2, 3 (Reference device), 4 and 5 μm shown in Table 1. Meanwhile, the channel width (W_f) and drift-region distance (DCG) of all devices were 300 μm and 57 um, respectively.

Third, the DCG distance values (shown in Figs.1 and 2) will be changed in order to find out the best parameter for ESD robustness. The device geometries of this Group-2 were as following: the channel length was 3 μm and the channel width was 300 μm. There are 5 different DCG's samples for testing, which were 57(Benchmark device), 62, 67, 72 and 77 μm listed in Table 2.

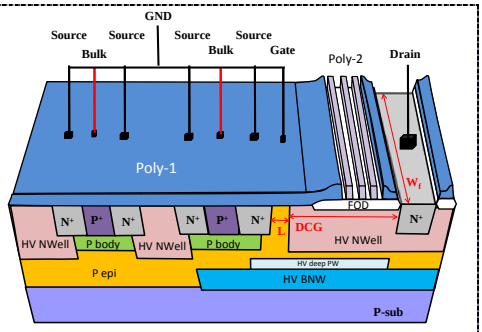

Figure 1. Cross-section view of a single-finger 600 V UHV nLDMOS.

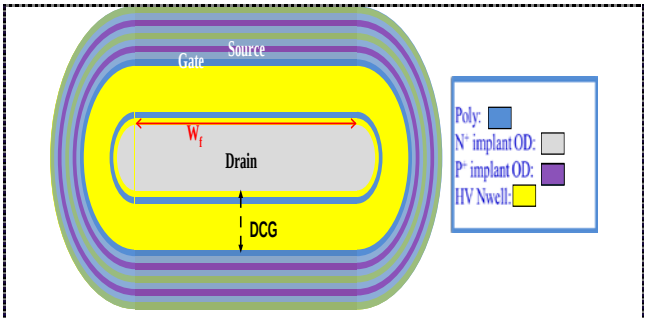

Figure 2. Layout diagram of a single-finger 600 V UHV nLDMOS.

	Cell name (unit: μm)
Type-1	nLD (L= 0.9)
Type-2	nLD (L= 2)
Type-3 (Ref. DUT)	nLD (L= 3)
Type-4	nLD (L= 4)
Type-5	nLD (L= 5)

Table 1. List of single-finger UHV nLDMOS DUTs by the L modulation.

Sample #	Cell Name	DCG (unit: μm)
Type-3	nLD_57 (Ref.)	57
Type-6	nLD_62	62
Type-7	nLD_67	67
Type-8	nLD_22	72
Type-9	nLD_77	77

Table 2. List of single-finger UHV nLDMOS DUTs by the DCG modulation.

2.2 Double-fingers UHV Cells

In Fig.3, the device parameters of the double-fingers 600V UHV Reference device cell were set to be: channel length L= 3 μm, unit-finger width (W_f)= 300 μm, drift-region distance (DCG)= 57 μm, finger number (M) is 2, so that total channel width W_{tot}= 600 μm.

And, the testing samples for double-fingers UHV cells were: (Group-3), the channel length was 3 μm and the total channel width was 600 μm, and there are 5 different DCG's samples for testing, which were 57 (Reference device), 62, 67, 72 and 77 μm, respectively. (Group-4), the channel length (L= 3 μm) and DCG width (57 μm) were fixed while the unit finger width (W_f) was modulated, which were 250, 300, 350, and 450 μm

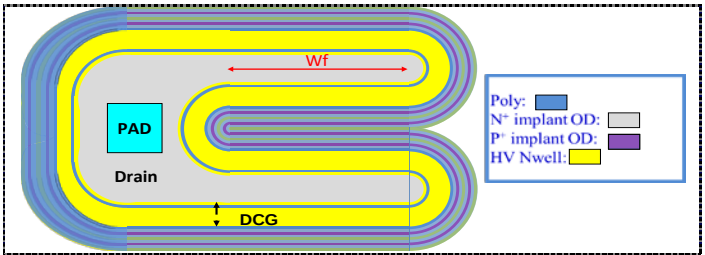

Figure 3. Layout diagram of double-fingers 600 V UHV nLDMOS.

3. MEASUREMENT RESULTS AND DISCUSSION

In terms of HBM ESD testing, a Keytek ESD testing machine was used, the test waveforms are being confirmed the MIL-STD-883 EOS/ESD test standard [13]. The test voltages for HBM test were in the range of ± 500 V to ±8000 V and changed ± 500-V per step.

3.1 single-finger UHV Cell

As Table 1 of the test components, the HBM testing results are listed and shown in Table 3 and Fig. 4. This channel-length modulation of group-1 600 V UHV nLDMOS devices will be at least passed HBM 3.5 kV during the positive-voltage zapping to VSS (PS mode), and the HBM immunity will be passed 8 kV as the negative-voltage zapping to VSS (NS mode) due to a parasitic forward-biased diode. Furthermore, as the test components shown in Table 2 (group-2), the HBM testing results are listed in Table 4 and Fig. 5. In the DCG modulation of 600 V UHV nLDMOS transistors, the HBM ESD robustness of positive voltage to VSS (PS mode) can pass minimum 6.75 kV, and which can be more than 8 kV under the negative-voltage zapping mode. As the DCG parameter increased, the parasitic high resistance in an UHV nLDMOS increased too. Therefore, the corresponding HBM immunity will be enhanced.

600V nLDMOS W= 300um, DCG=57um		**PS Mode (V)**	**NS Mode (V)**
L	**0.9 um**	5750	≧ 8000
	2 um	3500	≧ 8000
	3 um	6750	≧ 8000
	4 um	5000	≧ 8000
	5 um	5000	≧ 8000

Table 3. HBM robustness of a single-finger UHV nLDMOS DUTs by the L modulation.

600V nLDMOS W= 300um, DCG= 57um	PS mode (V)	NS mode (V)
nLD_Ref	6750	≧ 8000
nLD_62	≧ 8000	≧ 8000
nLD_67	≧ 8000	≧ 8000
nLD_72	≧ 8000	≧ 8000
nLD_77	≧ 8000	≧ 8000

Table 4. HBM robustness of the single-finger UHV nLDMOS DUTs by the DCG modulation.

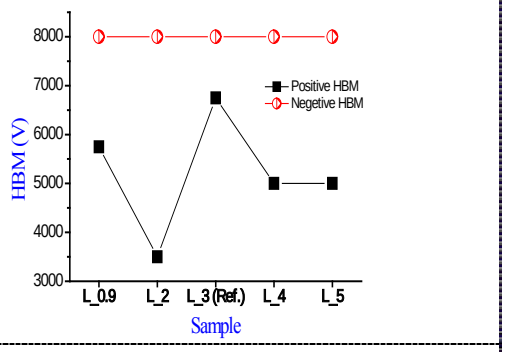

Figure 4. HBM ESD behaviours of a single-finger 600 V nLDMOS by the L modulation.

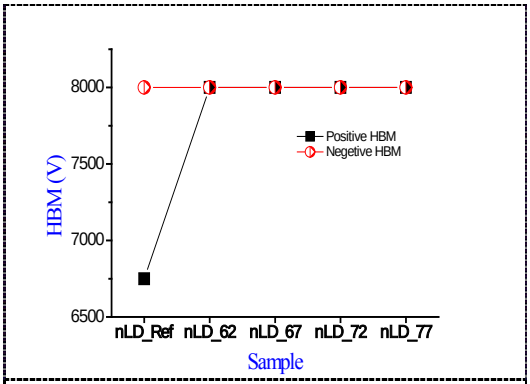

Figure 5. HBM ESD behaviours of a single-finger 600 V nLDMOS by the DCG modulation.

3.2 Double-fingers UHV Cells

First, from the HBM ESD zapping results of the Goup-3 samples, it could be obvious found that the positive anti-ESD ability was increased while increased the DCG width listed and shown in Table-5 and Fig. 6. Meanwhile, from the Goup-4 samples, the anti-ESD ability was increased as increasing the channel width. Overall, the positive anti-ESD ability can pass 2.75 kV as long as the DCG width over 57 μm. Next, as the test components of Group-4 samples, the HBM testing results are listed in Table 6 and Fig. 7. Then, in the DCG modulation of 600 V UHV nLDMOS transistors, the HBM ESD robustness of positive voltage to VSS (PS mode) can pass minimum 2.75 kV, and which can be more than 8 kV under the negative-voltage zapping mode. No matter the DCG width or channel width modulating, all of the gate-grounded nLDMOSs can be treated as a forward-bias diode, so that it can pass negative ESD 8 kV testing. Obviously, in the PS mode and as the W_f parameter increased, the ESD conducted width in an UHV nLDMOS increased too. Therefore, the corresponding HBM immunity will be linearly strengthened.

Table 5. HBM robustness of the double-fingers 600 V nLDMOS DUTs by the DCG modulation.

600V nLDMOS, L= 3μm, W_f= 300 μm	**PS mode (V)**	**NS mode (V)**
DCG-57 (Ref.)	4250	8000
DCG-62	2750	8000
DCG-67	4250	8000
DCG-72	4250	8000
DCG-77	6250	8000

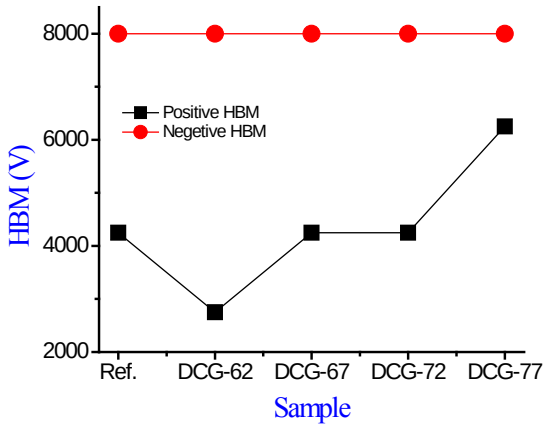

Figure 6. HBM ESD behaviours of a double-finger 600 V nLDMOS by the DCG modulation.

Table 6. HBM robustness of the double-fingers 600 V nLDMOS DUTs by the W modulation

600V nLDMOS, L= 3μm, DCG= 57 μm	**PS mode (V)**	**NS mode (V)**
W_f-250	3000	8000
W_f-300 (Ref.)	4250	8000
W_f-350	5000	8000
W_f-400	7750	8000

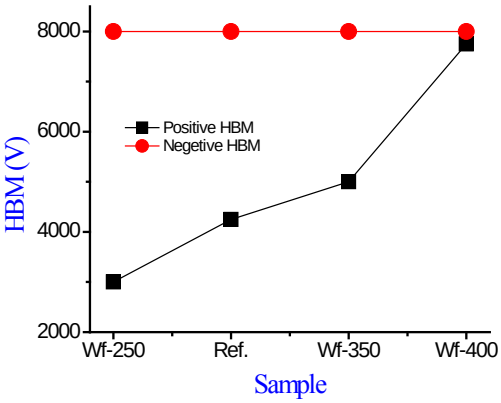

Figure 7. HBM ESD behaviours of double-fingers 600 V nLDMOS by the W modulation.

4. CONCLUSION

The proposed self-protected 600V UHV nLDMOS device exhibits good enough anti-HBM failure threshold under the Group-1~Group-4 layout designs. This paper allows a better understanding of modulations of channel length (L), drift-region distance (DCG), and unit-finger width (W_f) of a single-finger and double-fingers UHV nLDMOS devices in order to find out apposite layout parameters of these GGnMOS-form devices. Eventually, it can be found that the ESD capability is strongly correlated with the channel length (L), drift-region distance (DCG), and unit-finger width (W_f). Experimental data were shown that the HBM ESD robustness can be at least passed HBM 2.75 kV under the PS mode, In the NS mode zapping, all of the HBM robustness will be over 8 kV. Therefore, in order to optimize and improve the ESD robustness of UHV nLDMOS cells, these significant parameters should be validated through comprehensive to enhance its immunity efficiency.

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