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A 3.75Gbps Configurable Continuous Time Linear Equalizer and 3-tap Decision Feedback Equalizer in 65nm CMOS

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Abstract. This paper describes the design of the architecture and circuit block of the RX receiver's equalizer, which is used to reduce the inter-symbol-interference(ISI) in high-speed transmission backplane, and a 3,75Gbps configurable Continuous Time Linear Equalizer (CTLE) and 3-tap configurable Decision Feedback Equalizer (DFE) are designed and implemented in 65nm CMOS Technology. Those equalizer can be configured according to different channel conditions and the equalizer provides continuous operation range between 0.5Gbps-3.75Gbps, which are designed to work together to mitigate some or most of hte insertion loss and help the receiver to scale and optimize across different needs and applization. The simulation result shows that the horizontal eye opening of recovered data is 0.75UI at 3.75Gbps and the high frequency boost is up to 11dB.

Introduction

The increasing demand for high-bandwidth has been a challenge for system designers, which requires large numbers of I/Os per chip or higher data rates per I/O[1]. As we all know, the number of I/Os on systems couldn't scale proportionally with transistor count and logic capaciy, and I/Os must allow higher data rates to accommodate the demand for bandwidth, and high-speed serial interfaces are ideal for managing the high-speed data flow in and out of semiconductor devices. But, non-ideal channel characteristics often deteriorate the signal quality and cause inter-symbol interference(ISI) in received signal, which also causes difficulty in clock and data recovery (CDR) at high data rates and results higher BER[2]. And the channel-driven signal distortion increases with the serial signaling rate increases, while the bit sampling time needed to process this distortion only grows shorter, which limits the further increase of the I/Os' data rate.

The techniques used to compensate for signal distortion, therefore, become critical elements in the design, which includes two types of equalization schemes: one is at the transmitter side and usually called pre-emphasis; the other is at the receiver side and called equalization[2]. And this paper proposes architecture and circuit structures of the receiver equalizer, which contains a continuous-time liner equalizer (CTLE) and decision-feedback equalizers (DFEs). And the combations of those configurable equalizers can offer the best equalization capability for the main demanding backplane applications: the cutoff frequency and the gain of the CTLE, which can be viewed as high-pass filter, and the tap weights of the DFE are all programmable. The right combination fo CTLE and DFE can avoid the wrong frequency boost, amplify noise and compensated the channel conditions.

Background

A. Channel Insertion Loss and ISI

When signals travel through a link channel, the signal experience both attenuation and "distortion." This impact is referred to as channel insertion loss, and there is more channel loss for high-frequency components than low-frequency components. Thus, the link channel can be viewed as a low-pass

filter and high data rate pluses transmitted through the channel will broaden to greater than a unit interval (UI), which is usually referred as “inter-symbol interference”(ISI) [3].

B. RX Continuous Time Linear Equalization (CTLE)

Continuous Time Linear Equalization (CTLE) is one of the most popular linear equalization techniques at the receiver, and Figure 1shows the conceptual frequency response of the channel and CTLE and the result of the combination. As mentioned above, the link channel can be viewed as a low-pass filter. To compensate for the low-pass characteristics of the channel, the CTLE circuit is added at the receiver to achieve balance between the high-frequency and low-frequency components of the data stream, which can be viewed as a high-pass filter.

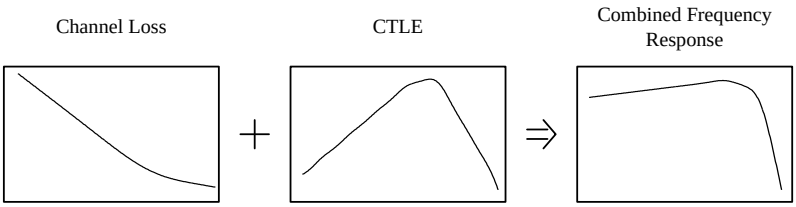


Figure 1. Frequency Domain Effects of CTLE

C. RX Decision Feedback Equalizer (DFE)

It is well known that linear equalization techniques, such as RX CTLE, have one major limitation: noise amplification. When noise is present on the channel, CTLE amplifies the high-frequency noise right along with the data. And Decision Feedback Equalization (DFE) is a equalization technique to mitigate inter-symbol interference (ISI) without amplifying noise. It works by directly removing the ISI from previous bits, allowing the current bit to be correctly sampled. And Figure 2 shows the block diagram of DFE[4].

$$y(t) = u(t) + \sum_{I=1}^{n} C_i \times y_d(t - i \times U.I.)$$

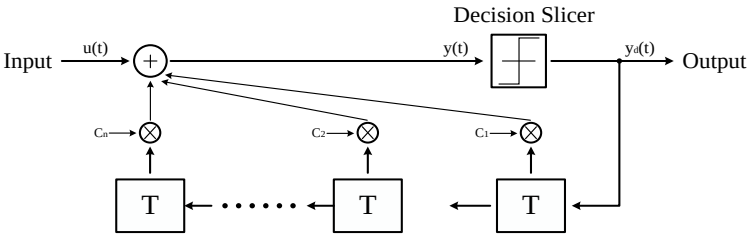


Figure 2. DFE Block Diagram

DFE starts with a “decision slicer” to determine whether the current symbol is High or Low. The resulting symbol goes through unit delays and multiplies with the tap weights. The weighted delayed signals are added together to the input analog signals[2].

Circuit Design

A. The architecture of Receiver Equalizer

As is shown in Figure 4, the receiver utlizes a CTLE followed by a summer , and a 3-tap DFE to reverse the channel loss, and the clock signals for CTLE and DFE blocks are provided by Clock generator, which is controled by the digital feedback signals of the CDR[5].

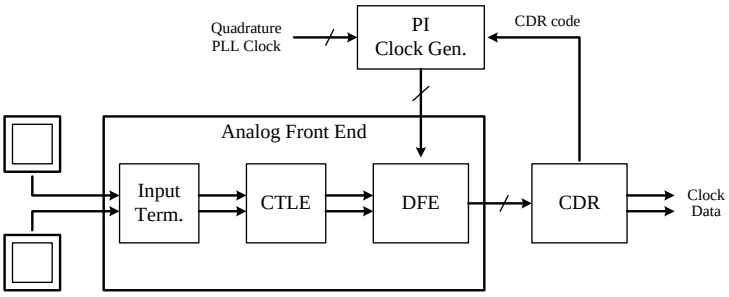


Figure 3. the architecture of Receiver Equalizer

B. CTLE Circuit Design

As shown in Figure 4, CTLE divides the signal path into two paths. One path uses a configurable single-pole high-pass filter to filter out low-frequency signals and amplify only the high-frequency components of incoming data. Another path is an wideband buffer to match the first path's time delay. Thus, the CTLE circuit can be viewed as a variant gain high pass filter, whose gain factor is equivalent to the ratio of the signal from the high-pass filter and the wideband buffer. At the same time, the CTLE circuit includes small AC-coupling capacitors that isolate the receiver from the line.

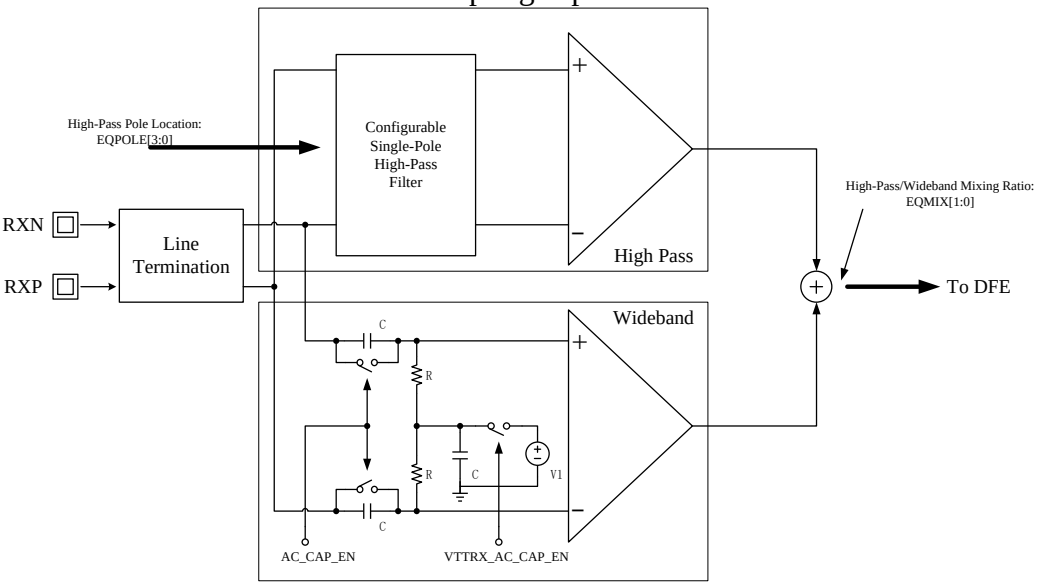


Figure 4. the architecture of CTLE

Shown in Figure 5(a), the high-pass filter of the CTLE circuit is a configurable RC passive filter, whose cutoff frequency is controlled by the EQPOLE port, which can be used to move the pole of the filter in the high-frequency path and the frequency range of the high-pass filter can be controlled. According to theFigure 6(c), the frequency response $H(j\omega)$of the high-pass filter is

$$H(j\omega) = \frac{R_{up}//R_{down}}{j\omega C + R_{up}//R_{down}}, \quad \text{whose pole is} \quad f_p = \frac{R_{up}//R_{down}}{2\pi C}.$$

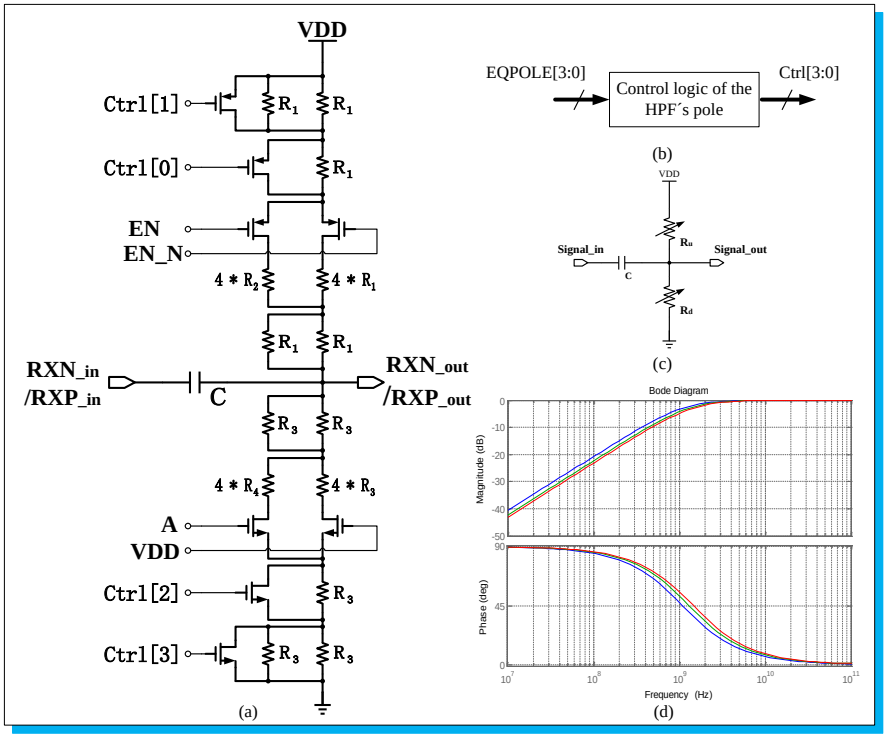
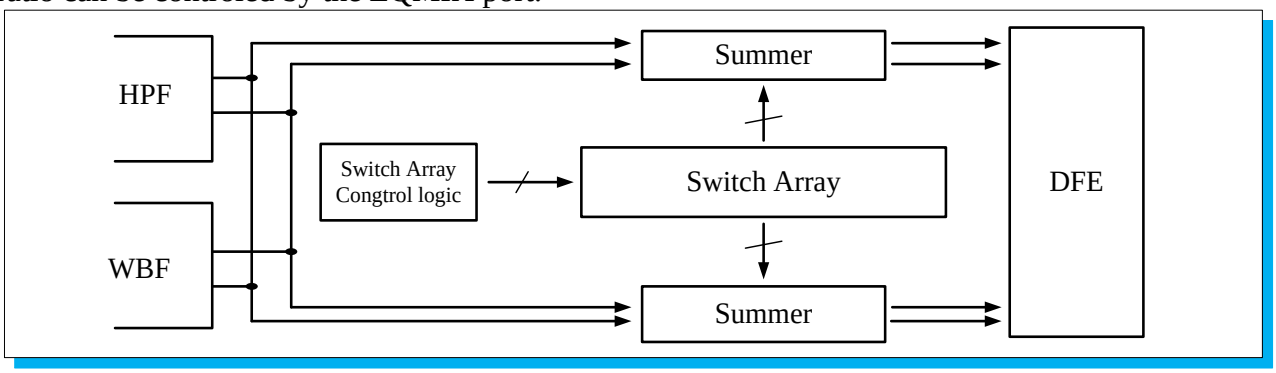
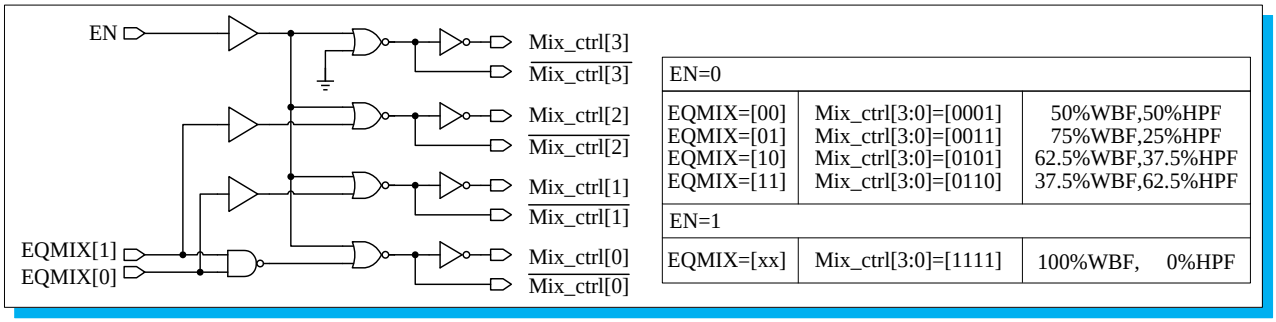


Figure 5. (a) the configurable high-pass filter circuit; (b) the control logic of the high-pass filter; (c) the simplified circuit structure of the high-pass filter; (d)the bode diagram of the high-pass filter.

The output signals of the high-pass filter and the wideband buffer are mixed by the configurable summer, which is based on current mode logic with resistive loads is shown in Figure 6 and can be used to produce a signal with amplified high-frequency components, and the high-pass/wideband mix ratio can be controled by the EQMIX port.

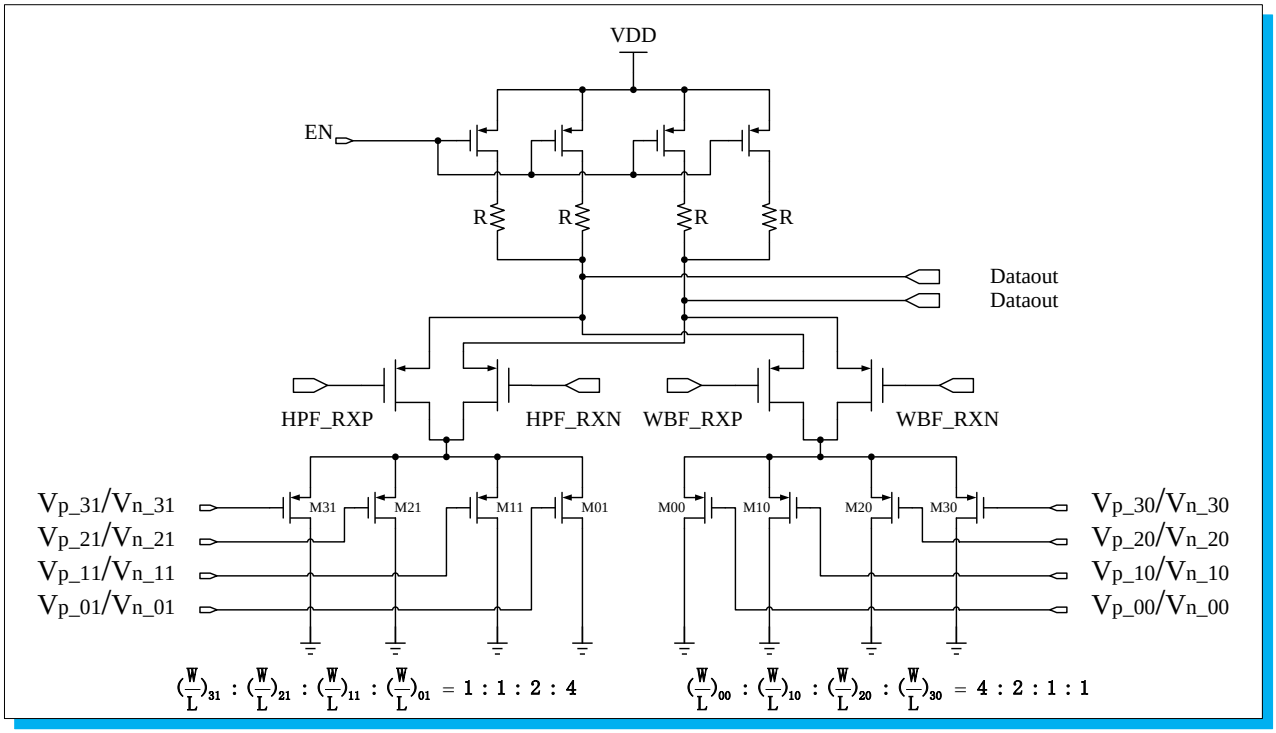


(a)



EN=0		
EQMIX=[00] EQMIX=[01] EQMIX=[10] EQMIX=[11]	Mix_ctrl[3:0]=[0001] Mix_ctrl[3:0]=[0011] Mix_ctrl[3:0]=[0101] Mix_ctrl[3:0]=[0110]	50%WBF,50%HPF 75%WBF,25%HPF 62.5%WBF,37.5%HPF 37.5%WBF,62.5%HPF
EN=1		
EQMIX=[xx]	Mix_ctrl[3:0]=[1111]	100%WBF, 0%HPF

(b)



(c)

Figure 6. (a) the architecture of CTLE's summer(b), the control logic of the summer and the relationship between EQMIX and the mix ratio; (c) the CML-based summer circuit

C. DFE Circuit Design

A quarter-rate DFE architecture is shown in Figure 7, each summer output is followed by a successice chain of three CML-based latches, which provied feedback to the three other summers. The quater-rate clkcks offset by 1-UI from each other, which is controled by the digtial feedback signal of the CDR. In each path, input data is sampled by a sample-and-hold(S/H) and added in a weighted fashion to the three previous bits[5][6][7][8].

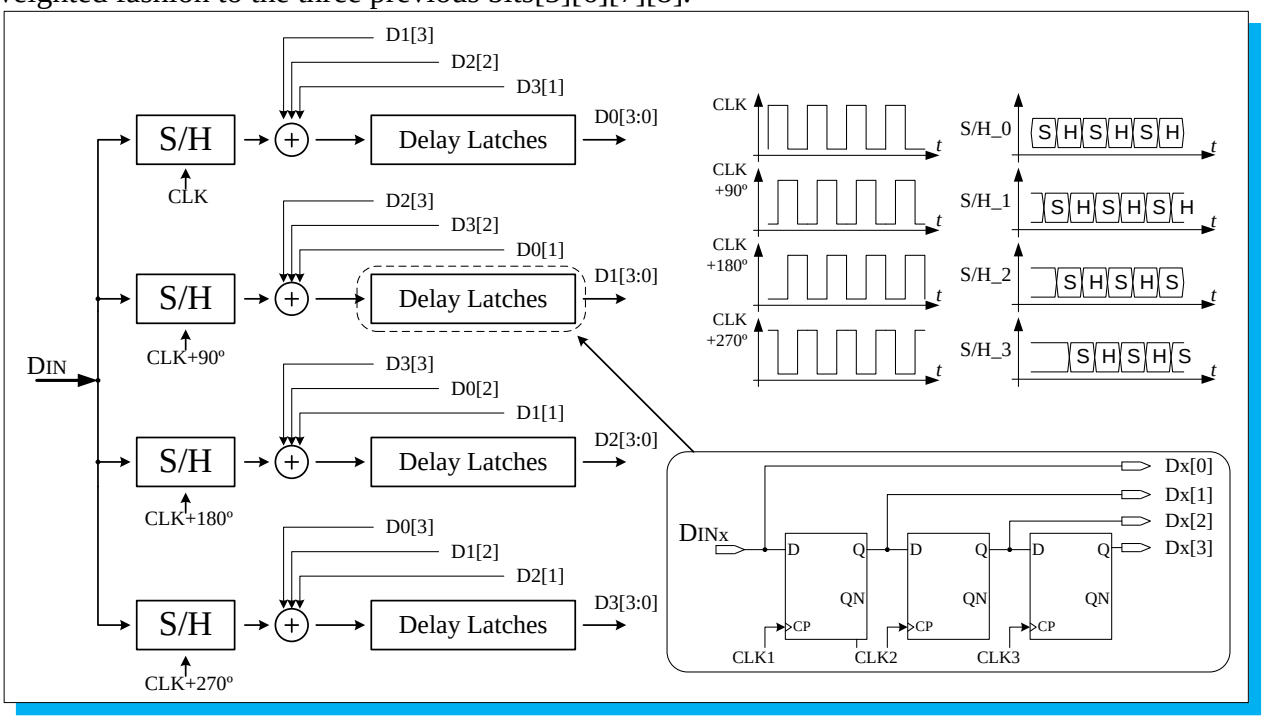


Figure 7. Block diagram and timing diagram of proposed DFE

Shown in Figure 8, the summer circuit consist of a main tap and three feedback taps, and the tap coefficients are control by current sources. According to different kinds of ISI signals, tap

coefficients can be modified to revover the signals. And a predrivers are be used at the input of DFE taps, which help the DFE tap achieves small gate delay and reduces output swing suitable for the proceeding differential pair. At the same time, the input common-mode waltage affects the speed and sensitivity of the summer circuit, and the output common-mode voltage also changes the current flowing through the DFE taps changes from channel to channel. Thus the common mode control logic is used to adjust the summer common mode to improve the performance of the DFE[1][5][6][7][8][9][10].

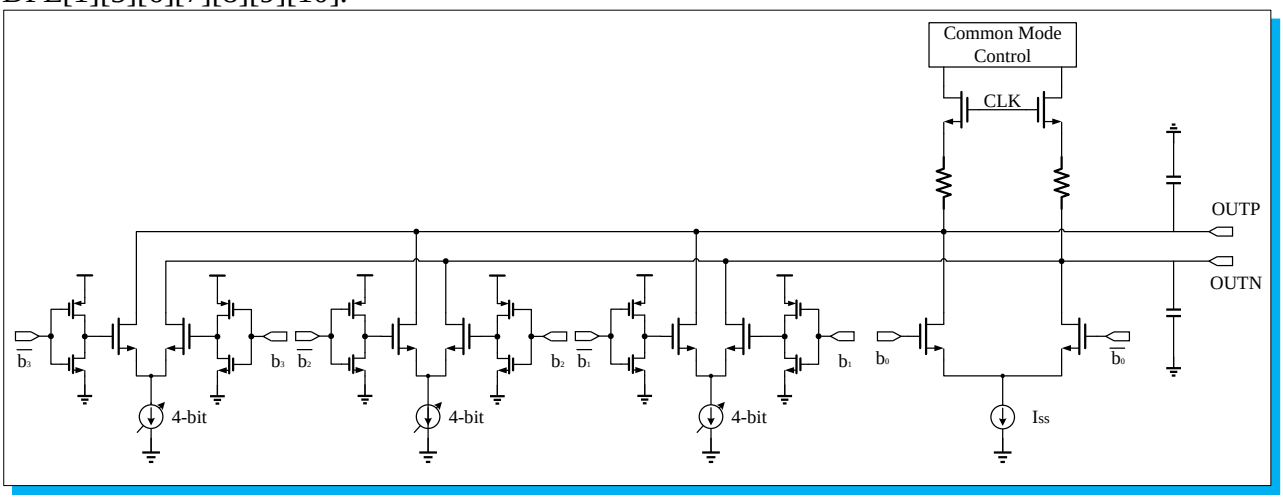


Figure 8. Summer circuit of the DFE

Figure 9 shows the S/H circuit, which consists of four comparators, four S-R latches and eight edgetriggered latches, which is trigeered by the same quarter-rate clock as the delay latches of DFE. When the clock signal CP is at high level, the S/H circuit samples the data from the CTLE; when the CP is at low level, the comparator is closed and the inputs of the S-R latch are at high level, which help the S/H circuit to remain the output result of the comparator.

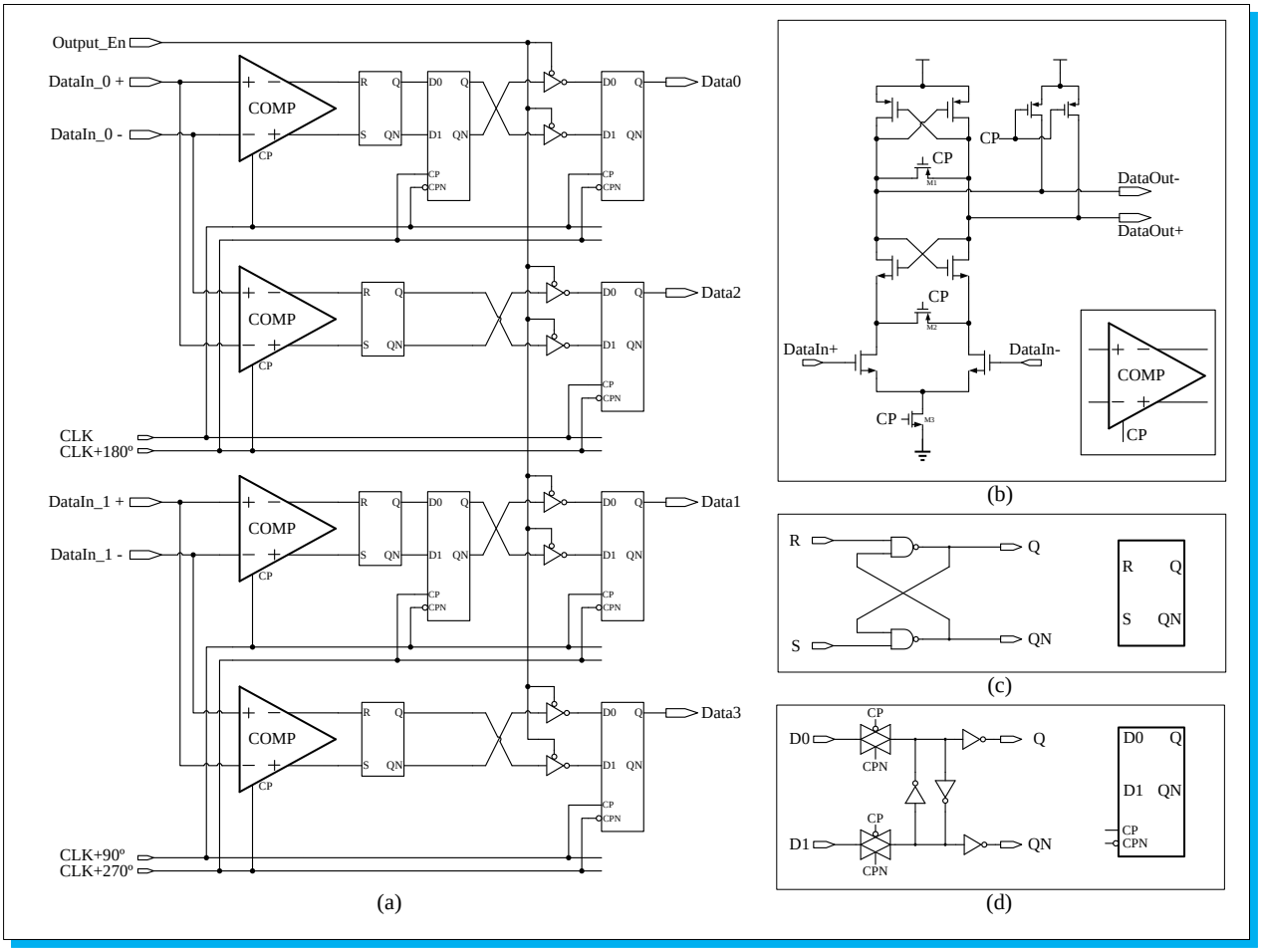
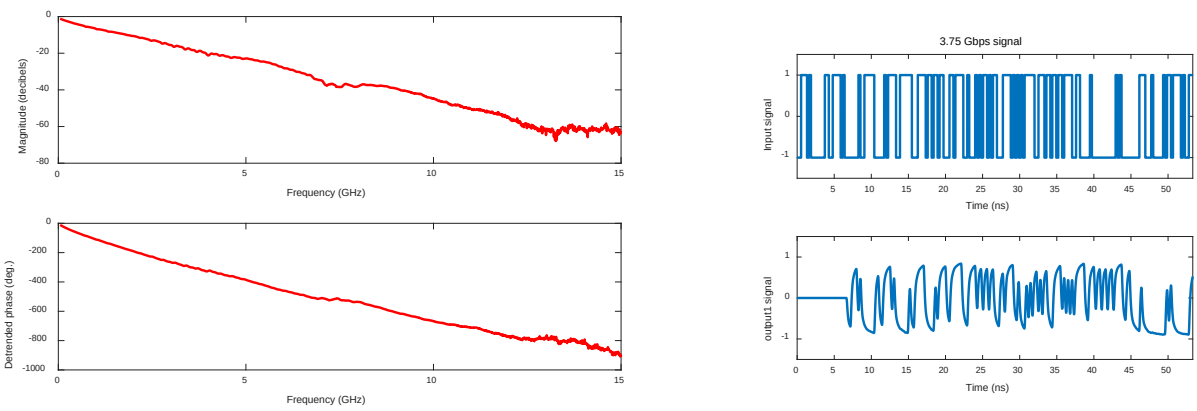


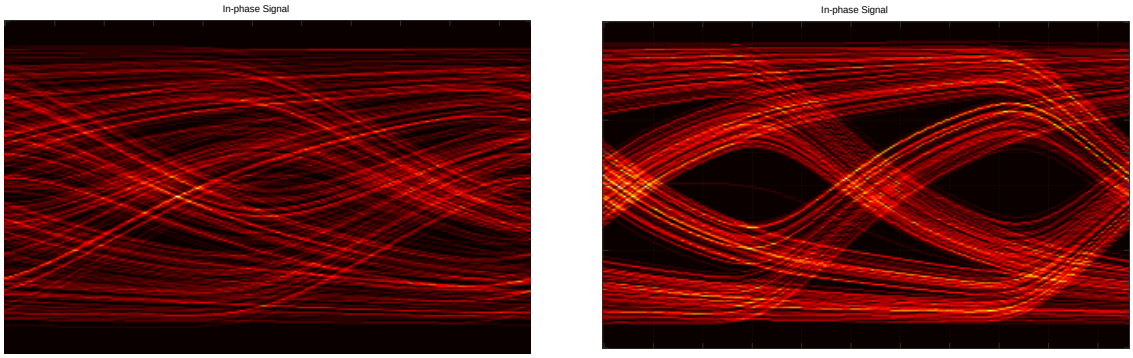
Figure 9. S/H circuit

Simulations and Conclusions

Figure 10 is the post simulation result, where Figure 10(a) is the channel frequency response of the PCB trace, Figure 10(b) is the waveform of the input signal of the channel and the output signal with ISI from top to down, Figure 10(c) and (d) are the eye diagram of the received siganl and equalizer recovered signal. It can be seen that the eye is opened well compared withe the received signal and the horizontal eye opening is about 0.71U.I. at the rate of 3.75Gbps. When the RX equalizer only contain CTLE, the mean periodic jitter is 0.34U.I., and the high frequency boost is up to 6dB at the rate of 3.75Gbps; when the RX equalizer contain CTLE and DFE, the mean periodic jitter is 0.27U.I., and the high frequency boost is up to 11dB.



(a) (b)



(c) (d)

Figure 10.Post simulation results

In this paper, Continuous Time Linear Equalizer (CTLE) and 3-tap Decision Feedback Equalizer (DFE) are designed and implemented in 65 CMOS Technology. The equalizer can be configured according to different channel conditions and the equalizer provides continuous operation range between 0.5Gbps-3.75Gbps and the simulation result shows that the horizontal eye opening of recovered data is 0.75UI at 3.75Gbps.

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