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Design of Digital Switching Power Supply Based on FPGA

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Abstract. With the development of power electronic technology, the control technology of power electronic device is becoming more and more complicated. The switching power supply is a indispensable component in modern power electronic equipment. Its quality and size have a direct impact on the whole performance of electronic equipment. Digital control technology and the applications of FPGA have become a new research hotspot in the field of power electronics. Digital control can reduce the aging of the device and the impact of temperature drift on the accuracy of the convenient. This paper studies the digital switching power supply based on FPGA and points out the system structure of the system.

Introduction

In the current market, switching power supply products are basically used PWM integrated circuit control circuit switch on and off. Texas Instruments (TI) and the United States Microchip (Microchip), represented by the power chip production giant, developed a large number of dedicated power control chip, the use of a dedicated power supply control chip, its flexibility, scalability And programmable capabilities are greatly limited. In order to complete the more complex power control, at the end of the last century many domestic and foreign universities and colleges began to SCM (single-chip microcomputer), digital signal processor (DSP) applied to the switching power supply, and achieved the corresponding results. For example, the literature on the application of single-chip power in the study done, literature on the DSP applied to the switching power supply was introduced. TI has also developed S320C2000 series DSPs and DSP development kits for digital power supplies to enable developers to use the DSPs for digital power development, facilitating and speeding up DSP-based digital switching power supply R & D processes. There are also some people apply ARM digital switching power supply design.

Switching Power Supply Topology

According to the switching power supply output type, it can usually be divided into two kinds: DC and AC, DC switching power supply topology is to be discussed in this paper. Isolated topology includes Fly-back and Forward architecture, Half Bridge and Full Bridge architecture. It can be divided into two types: isolated and non-isolated according to whether the topology is electrically isolated or not. Push-pull (Push-Pull) structure, in addition to the forward structure of the formation of the double forward (Switches Forward) and Active Clamp Forward (Active Clamp Forward) structure is also widely used, non-isolated, including Buck, Boost, Buck-Boost, Cuk, Zeta, Sepic.

Push-pull topology drive circuit is relatively simple, the use of the two power tube turns on, the transformer side of the center-tap structure, relative to the full-bridge inverter circuit is the same input voltage to the switch device voltage The requirements are twice that of the latter, so the push-pull structure in the DC low-voltage input applications are more suitable, and push-pull structure of the transformer core is also easier magnetic saturation.

Half-bridge topology use less IGBT/MOSFET devices, relatively simple circuit structure, so a wide range of applications, but compared with the full-bridge topology, input power is under the same conditions, the input power transformer only half of the amplitude of the exchange square wave, So the equivalent power under the half-bridge circuit switch rated current to achieve the latter

two times the power switch. If the combination of the two inverter half-bridge circuit to form a full-bridge topology of the inverter circuit, which compromise the advantages of half-bridge circuit, and transformer utilization higher than the half-bridge, suitable for high-power use. In summary, the power supply in this paper selects the full-bridge inverter topology, and then considers that the power output is a low-voltage and large-current DC type, so the output side adopts full-wave rectification.

Switching Power Supply Main Parameter Design

Parameter tuning is actually in accordance with certain guidelines to adjust the target parameter value, so that it matches the characteristics of the controlled object, the control system response to meet the design requirements. Among the many control strategies, PID control is one of the earliest developed and widely used, the most classical control algorithm, PID control has the advantages of simple algorithm, good adaptability of the robustness and high reliability. The PID controller model considers three factors: system error (P), past (I), and future (D), so the control performance is better. It has been tested in a large number of engineering practices. 10 control algorithm to achieve analog and digital implementation of the points, the use of analog circuits to build the realization of the analog PID controller, the use of software programming method (digital method) called digital PID controller, digital PID parameter modification does not require analog PID. The digital circuit modify does to need to modify the circuit, but only a simple software to modify the operation, whci is flexible and has convenient high precision.

In the field of industrial control, some of the controlled object in the previous summary has been more clear for such systems generally PID parameter selection is appropriate, the control effect is better, even for a less certain system, because of its good of the robust adaptability, the control effect is often satisfactory.

Although the pro algorithm is the most important of the three parameters, but let engineers feel the headache is also the setting of these three parameters, very early at home and abroad on the PID parameter tuning method to do a lot of research, in general: a The other is based on the basic mathematical model of the controlled object using a certain method of setting parameters, after the test in the field to make the necessary amendments. The other is based on the experience of the engineers to give their own experience and then modify the parameters of repeated testing.

It should be noted that the PID parameters based on the pole assignment method are based on the theoretical mathematical model, since the model is obtained under a limited set of conditions, the model can not be fully consistent with the actual, so the parameters based on model tuning may make the control effect not Ideal, the need to adjust the actual response to the system PID parameters, the system to achieve the desired results. The above method is also commonly used by engineers, but the PID parameters need to have the direction of the target adjustment, otherwise it will waste a lot of time not get a good effect, you can refer to the experimental PID tuning method based on following analysis.

In addition, the switching power supply more or less contains some high-frequency voice, too much differential effect may cause serious interference, so be careful to use the differential effect, a reasonable choice of differential value, not too much. If the interference is too large in the actual test, you can cancel the differential effect, namely the differential coefficient IC taken as 0, using the H-structure controller. The same PI controller has parameters, but also according to the experimental results continues to be amended, benzene to obtain satisfactory control results.

Switching Power Supply to Achieve the Main Hardware Circuit

Traditional high-frequency switching power supply control circuit from a number of discrete components to build up, these discrete devices aging over time, there is the inevitable temperature drift phenomenon, thus reducing the accuracy and reliability of power supply. In this paper, FPGA-based digital power supply, the control part of the data operation, logic output, and the host computer communication is done by the FPGA to reduce the control part of the use of discrete

components to improve the stability of the power supply and technical confidentiality.

Control circuit is the core part of the FPGA, FPGA ADC clock to provide work at the same time the incoming data into the ADC processing, after a certain logic operation output control signal to complete the power of closed-loop control. The design of the FPGA is cost-effective EP2C8Q208C8 and EP2C8Q208C8 is Altera's Cyclone II generation FPGA. EP2C8Q208C8 internal power supply is 1.2V and its embedded multiplier resources in the implementation of multiplication can greatly reduce the FPGA LE valuable resources. PLL module can easily achieve the clock frequency, frequency, phase shift function, and the output clock signal is relatively stable, PLL multiplier function in the generation of high-precision digital PWM has important applications.

EP2C8Q208C8 normal work, the configuration data stored in the internal SRAM, SRAM configuration information in the system will be lost after power outage, so the need for external serial configuration chip, chip configuration after power-off chip will be reloaded to the FPGA internal, Then all the input/output pins and internal registers initialized, after initialization into the user mode.

There are three configuration options for the FPGA, passive configuration mode (PS), active configuration mode (AS) and the most widely used JTAG configuration mode. The PS is an external controller that configures the FPGA as a memory and uses the enhanced device to complete the configuration process and is suitable for all Altera series FPGAs. JTAG is an industry-standard interface and almost all of the Altera series FPGA can use the JTAG interface to complete the configuration. This control board adopts AS and JTAG two kinds of interface way.

In order to reduce the ADC output delay to the FPGA path, reducing the main circuit of the ADC circuit of the electromagnetic interference in the design of the circuit board when the ADC circuit integrated into the control circuit board to detect the circuit board over the two current and voltage signals, After ADC sampling and sent to the FPGA for processing.

RS232C communication protocol standard is the United States Electronic Industries Association (EIA) and Bell (BELL) and other companies with the development of the standard serial interface on the form of communication, electrical characteristics and signal line functions are clearly defined. The RS232C standard and the general logic 1 represent the high logic. 0 represents the low level. It defines the negative level-3 -15V as the logic "1" and the positive level + 3 ~ + 15V as the logic "0". In order to match the logic level of the interface and the TTL device, it is necessary to convert the logic level specified by RS232C. The MAX232 level conversion chip of Maxim is used in this design.

In order to prevent the external interference signal from sneaking into the control board to affect the work of FPGA circuit, a digital isolation chip ADUM1412 is used to isolate the external signal from the FPGA internal signal and improve the anti-interference of the circuit. The ADUM1412 isolator operates from a supply voltage of 2.7 V to 5.5 V and has four independent isolated channels that support multiple channel configurations and data rates up to 10 Mbps.

Digital Power Supply Software Construction

Digital controller based on FPGA switching power supply mainly includes several units: data acquisition and filter processing, digital compensator implementation, ZVZCS digital PWM drive wave generation, host computer communication module, protection and status display control module. FPGA programming using the Quartus II 11.0 environment, the simulation environment is ModelSim 6.5e, the programming language is used in Verilog HDL 2001. Although verilog grammar in many places and C language are similar, but the preparation of Verilog program thinking and C language is different: Verilog program embodied in the FPGA is parallel execution, completely different from the C language serial execution rules, Verilog The description of the hardware circuit, we must ensure that the syntax used to be integrated into the actual circuit, and C is a process-oriented software programming language, does not correspond to the actual application circuit, the general syntax statement can be C compiler identification, The code or machine code is executed by the CPU.

ADC collected voltage and current data contains a certain high-frequency and low-frequency

harmonics, in particular, high-frequency switching switch and rectifier diode reverse recovery will affect the detection circuit output. Digital filter has reduced the cost of hardware, good stability, high reliability, there is no impedance matching problem, FPGA has the high-speed characteristics of high-speed digital signal processing circuit, , In a very short period of time to complete the digital filter, reducing the digital filter to bring the system response delay characteristics. Commonly used digital filtering methods are limiting filtering, median filtering, arithmetic mean filtering, HR filtering. The filter can effectively reduce the random interference and peak pulse interference, it can not suppress the periodic interference, smoothness is relatively poor, median filter can effectively weaken the interference caused by accidental factors, but its processing more filtering The speed is relatively slow, not suitable for rapid dynamic response of the occasion, arithmetic mean filter using a very wide range, it can suppress the general random interference and smoothness is also better.

Conclusion

In the power control, this paper uses the FPGA as the main controller of the program to complete the power of all-digital control. FPGA control ADC for voltage and current data acquisition and digital filtering, then sent to the digital controller module to complete the operation process and make the output duty cycle value. DPWM module input is duty cycle, in the DPWM module, it complete the relevant logic operations, resulting in limited bipolar drive waveform. In communication, it makes the provisions of the FPGA and the host computer's RS232 communication protocol and frame processing methods, so that the host computer can control the value of a given FPGA register to complete the output of the automatic adjustment, while the host computer interface shows the next bit machine voltage and current information. Those processes method and system construction in this paper should have much meaningful value in the FPGA power supply design.

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