Design of code error detector based on FPGA

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Abstract. With the development of social productivity and the improvement of people's living standard, the development of modern computer technology is more and more fast. In the communication system, the code error detector is the important equipment to detect reliability of communication system, and the traditional code error detector is based on collaborative work of CPLD and CPU[1], not only is the structure complex, expensive, but it is inconvenient to carry. Code error detector based on FPGA, using FPGA to complete the integration of design of control and test module, to improve the scalability and integration of the system. This paper is based on principle of M sequence generation and code error detection, using the VHDL hardware description language, to realize the design of a simple bit by bit comparison code error detector and the simulation of each function module.

INTRODUCTION

With the rapid development of information, communication has become an indispensable part of people's life, the digital communication network has penetrated and influenced every aspect of our daily lives, people have felt the convenience brought by the network communication, in addition to the Internet that we are familiar with, the backbone communication network like telephone network is also more and more applied to all walks of life. Digital communication that has strong anti-interference ability, high quality of long distance transmission, good convenience to connect with computer, easy encryption and other advantages has become an important means of modern information transmission [2]. With the wide application of large scale integrated circuit, digital communication has developed rapidly, at the same time, the reliability of transmission is particularly important

At present, the most of error code detector sale on market can only be tested the standard communication channels of the telecom department, they are expensive with larger volume, and cannot be used for the dedicated channel that exists in a large number of practical work or the channels set up by own selves (such as for weather forecasting, hydrological monitoring and other special purpose). The bit by bit comparison code error rate detector in this paper take the special consideration in the test requirements of dedicated channel or channels set up by themselves when they are designed. It is designed based on FPGA, which has small volume, and the cost is low, it can be used for error code test on the standard communication channel, dedicated channel or channels set up by themselves, which has high practical value and market value.

PSEUDO RANDOM SEQUENCE AND ERROR DETECTOR

A. Brief introduction of pseudo random sequence

Pseudo random sequence or pseudo random code, a code is a random characteristic of imitation random sequence generation, also known as pseudo noise sequence or pseudo noise code. In digital communication, pseudo random sequence. There are many kinds of communication in engineering applications, often using binary pseudo random sequence, the sequence only "0" and "1". Two kinds of binary pseudorandom sequences is generally through the shift register and feedback circuit

together to produce. The feedback shift register can be divided into linear feedback and nonlinear feedback shift register two. Which consists of a linear feedback shift register sequence of binary digits' cycle produced the longest is called the maximum length linear feedback shift register sequences, also known as the m sequence.

B. Error detection

Whether it is equipment failure, propagation fading, inter symbol interference, adjacent channel interference and other factors may cause deterioration of system performance and even cause communication interrupt[3], the result can be through the error forms. About digital communication receiver, the decision circuit is indispensable, causing error in judgment of the basic reasons can be summarized as the following several points:

a) The deviation of the decision level caused the miscarriage of justice;

b) Sampling time offset caused by miscarriage of justice;

c) Superimposed noise caused by miscarriage of justice.

CODE ERROR DETECTOR DESIGN

Bit by bit compare the basic principle of the type of error code detector is will by the transmitter and receiver of the two columns of the same type of sequence after synchronization symbols one by one are compared, if there is an error, then two lines of code in the sequence have the same symbol will become different using this kind of difference, in the control of clock synchronization by XOR gate one by one symbol is compared, will compare the results through the counter is sent to the display circuit to display. The block diagram as shown in Figure 1.
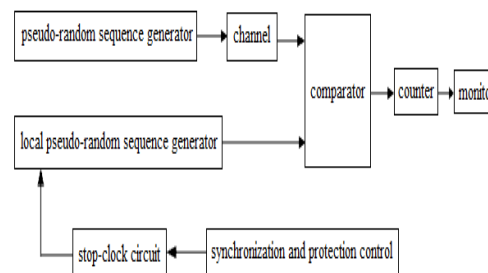

Figure1   simpe bit by bit comparison code error detector

Pseudo random sequence is shifted in the clock under control, if the local PN sequence and receiving PN sequence synchronization. It can not achieve the correct comparison, two sequences therefore, first extraction of bit synchronous signal from the received sequence. The stop buckle clock circuit function is when the corresponding sequence of States is not the same, namely state synchronization, synchronization and protection circuit outputs a control signal through the stop button clock circuit excluding a clock pulse[4].

Even the "1" counter and output control circuit has two functions: one is to count the comparator output state even the "1" state, the number when the counter reaches the set value, the counter output is "1", and "parallel control input and state control circuit, the output of the parallel position" 0 ", so that the input state comparator are" 0 ", the output is" 1 ", said the state has synchronization; if the state is not synchronized, even the" 1 "of the output of the counter is always" 0 ". Even the other function of" 1 "counter when it is lost that is" 1 ", to make the error counter. If the whole system is synchronous, the state step, even the" 1 "counter controlled by the output state error statistics and the threshold detection circuit in the graph. If the two m sequences are not synchronized, the comparator is given by the loss build step The error, according to the characteristics of m sequence, the bit error rate (BER) is 0.5. Error threshold detection circuit through error threshold is used to recognition sequence is out of step, if the state lost step, error detector output low level, even "1" counter reset, the system enters to capture state [5]. Jane to a single bit error device specific model diagram as shown in Figure 2.
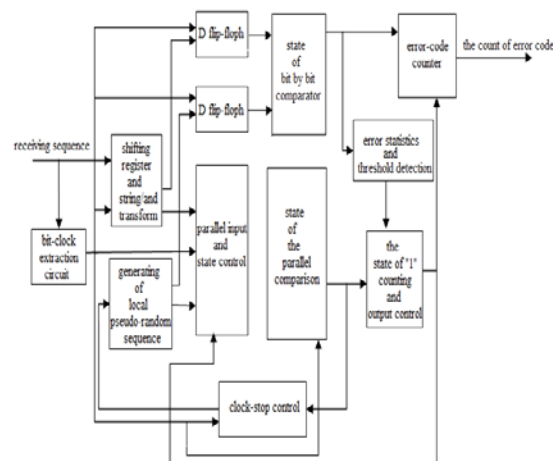
Figure 2simple code error detection model

ERROR DETECTOR MODULE SIMULATION

A. Shift and string / and transform modules

In the design of error code detector, using four shift register to the receiving sequence of shift and on / and transform. The specific work process: in clock CLK rising edge triggered under, from InP input receiving m sequence, according to the order of InP, A3, A2, A1, A0 to shift, but at the same time, the A3, A2, A1, and the output of the A0 respectively, the output of B3, B2, B1, B0 end, thus completing the string and transform function Q end signal from A0 output end, as a shift of 4 bits of serial m sequence signal. The timing simulation as shown in Figure 3.
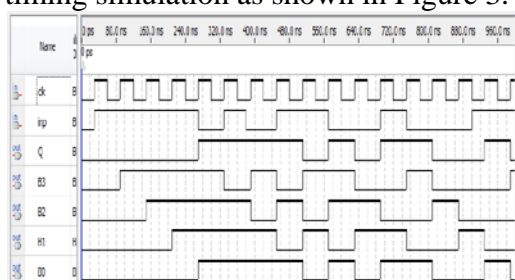

Figure 3   Time series simulation waveforms of shift and series / parallel transform

B. Bit by bit comparison module

By simple error model shows, receiving and local sequence respectively after shaping of D flip flops is then fed into a bitwise comparison module. By bit comparator is designed at the rising edge of the clock "CLK0" arrival, if the comparison control signal "en" = "1", a sequence of paths and b order column is bitwise XOR comparison, from the end of a Z output the results. The timing simulation as shown in Figure 4.
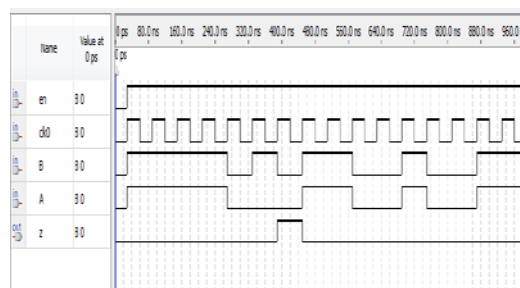

Figure 4   Time sequence simulation waveform of bit by bit comparator

Conclusion

Error detector is designed in this paper based on FPGA, the error detector has a better ability to upgrade and portability. We in based on FPGA based on the Verilog language programming, the MCU control part using C language, the error is with small volume, low cost and the characteristics, his innovation is since the start of the m sequence generator, bit synchronization module and sequence synchronization module. With continuous improvement and improve the bit error rate (BER) an external detector, it will more professional users with more comprehensive and better quality of service and support.

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