The study on a novel Buck-Boost DC-DC converter

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Abstract. In this paper, a novel topology of DC-DC converter is proposed. The working principle of the new topology is analyzed, and the voltage relation of each part of the circuit is deduced. And the comparison with the Z source DC-DC converter is performed, the feasibility and advantages of the new DC-DC converter topology are verified by working principle analysis, parameter design and circuit simulation.

Keywords: new topology; Z-source DC-DC converter; advantages.

1 Introduction

With the rapid development of electronic technology, the relationship between power electronic equipment and people's work is becoming more and more closely, and the electronic equipment cannot be separated from the power supply. Due to its small size, light weight, low power consumption, high efficiency and wide voltage regulation range, the switching power supply has been widely used in various fields.

Traditional power supply mainly includes Boost, Buck, Buck-Boost circuit, people have made remarkable achievements in the research of traditional power supply[1]. However, due to the disadvantages of the topology itself, the development of switching power supply is hindered. Electromagnetic interference easily lead to circuit fault; the existence of dead time can make the discontinuous input current, input and output current has pulsation, thus the distortion rate of the output voltage and the negative effect on the load are increased; switching transistor emitter is not Common-grounded, the drive circuit is complex. Therefore, in some occasions, the traditional switching power supply topology cannot meet the application requirements.

In order to improve the topology and the performance of the system, Z-source circuit [2] has been widely studied. Z-source converter, which is constructed by impedance network, has simple structure and high voltage gain, which can effectively reduce the power conversion stages and improve the performance of the whole system. But the traditional Z-source DC-DC converter has some defects: the input current is discontinuous, which causes the output voltage drop in the non straight mode; Only provide boost but not buck function, and the boost capacity is limited; capacitors C_1 and C_2 bear the same voltage stress and are higher than the input voltage V_0, the selection freedom of the impedance network parameters is limited. Therefore, the traditional Z-source converter needs to be modified.

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This paper presents a new type of DC-DC converter circuit, by analyzing the working principle, and discussing the work mode of the circuit, and then through simulation to verify the correctness of the derivation.

2 Circuit topology and working principle

The main circuit of the novel converter topology is constituted by two inductors L_1, L_2 and two capacitors C_1, C_2, and two bidirectional power switches S_1 and S_2 are alternately triggered in a complementary manner, by varying the duty cycle of the PWM control signal of the power switches S1, S2, the output voltage could be regulated. The charge and discharge of the energy storing devices, that is, the two inductors and the two capacitors can provide the Buck-Boost function. Circuit topology is shown in Figure 1.

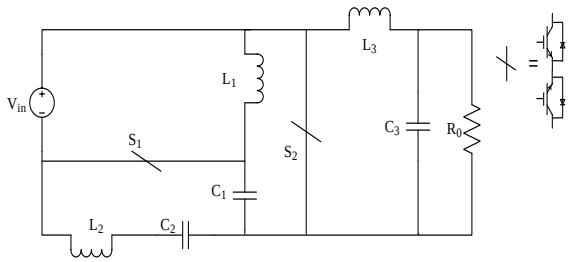
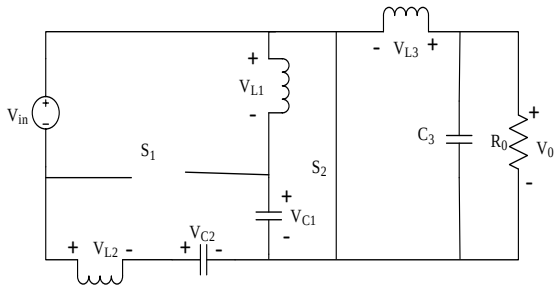


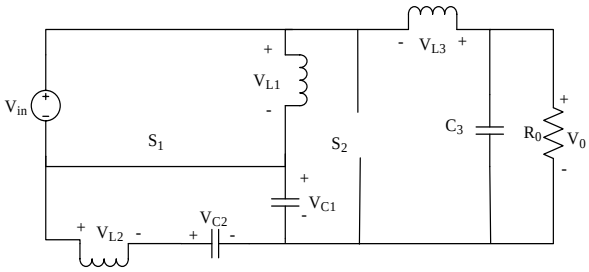
Figure 1. Circuit topology of a novel DC-DC converter

2.1 Working principle

Same to the (quasi) Z-source DC-DC converter[3-5], the proposed converter is also divided into two working conditions, by controlling the duty cycle of the switch to achieve the Buck-Boost function. Its equivalent circuit diagram is shown in figure 2.



(a) working states 1 (S_1 off, S_2 on)



(b) working states 2 (S_1 on, S_2 off)

Figure 2. The two working states of the new circuit

Assuming that in a switching cycle T, the switch S_2 is turned on, that is, the time interval of state 1 is T_0, from the equivalent circuit diagram 2 (a) can get the following formula:

$$v_{L1} = -V_{C1} \tag{1}$$

$$v_{L2} = -V_{C2} - V_{in} \tag{2}$$

$$V_0 = v_{L3} \tag{3}$$

Assuming that in a switching period, the time interval of state 2 is T_1, from the equivalent circuit diagram 2 (b) can get the following formula:

$$v_{L1} = V_{in} \tag{4}$$

$$v_{L2} = V_{C1} - V_{C2} \tag{5}$$

$$V_0 = v_{L1} + V_{C1} + v_{L3} \tag{6}$$

In a switching period T, the average voltage of the inductor should be zero, that is, $V_L = \overline{v_L} = 0$. From formula (1), (4) and (2), (5), we have

$$V_{L1} = \overline{v_{L1}} = \frac{-V_{C1}T_0 + V_{in}T_1}{T} = 0 \tag{7}$$

$$V_{L2} = \overline{v_{L2}} = \frac{(-V_{C2} - V_{in})T_0 + (V_{C1} - V_{C2})T_1}{T} = 0 \tag{8}$$

From formula (7) and (8), we have

$$V_{C1} = \frac{1-D}{D} V_{in} \tag{9}$$

$$V_{C2} = \frac{1-2D}{D} V_{in} \tag{10}$$

Where D is the duty cycle of the switch S_2, $D = \frac{T_0}{T}$.

From formula (3) and (6), we have

$$V_{L3} = \overline{v_{l3}} = \frac{V_0 T_0 + (V_0 - V_{in} - V_{C1})T_1}{T} = 0 \tag{11}$$

$$V_0 = \frac{1-D}{D} V_{in} \tag{12}$$

In the formula: $B = \frac{1-D}{D}$ ($0 < D < 1$) is the voltage gain of the new topology. When $D < 0.5$, the topology has boost function and with the increase of D, the voltage gain is decrease; when $D > 0.5$, the topology has buck function and with the increase of D, the voltage gain is increase.

Compared with the traditional DC-DC converter and the traditional impedance network, the new converter is easy to get a larger voltage gain, which can improve the efficiency of energy conversion.

The relationship (the traditional Z-source converter and the new converter)between the voltage gain B and the duty cycle D is shown in Figure 3.

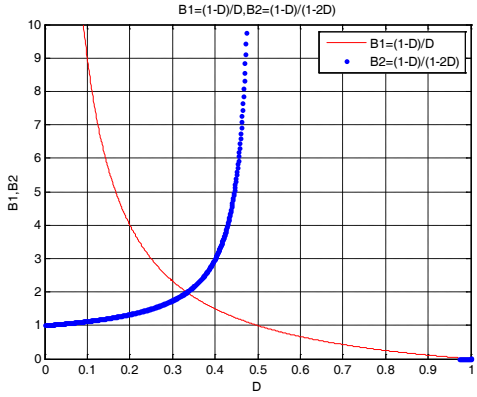


Figure 3. The relationship between the voltage gain B and the duty cycle D

(B_1 is the voltage gain of the proposed topology; B_2 is the voltage gain of the traditional Z-source DC-DC topology)

2.2 Working modes

After the system is in stable state, the circuit begins to work periodically. Reference directions of voltage and current are shown in Figure 2 and Figure 3. If the inductance is large enough, the working process of continuous mode only discussed here (current of inductor L1 is not reverse).

In the continuous mode, according to the working process of the circuit and the current changes of the inductor L_2, it is divided into four kinds of working states, in the working state 1, the current commutation of inductor L_2 corresponds to two working modes;

In the working state 2, the current commutation of the inductor L_2 is corresponding to the other two kinds of working modes. The equivalent circuit diagram is shown in Figure 4.

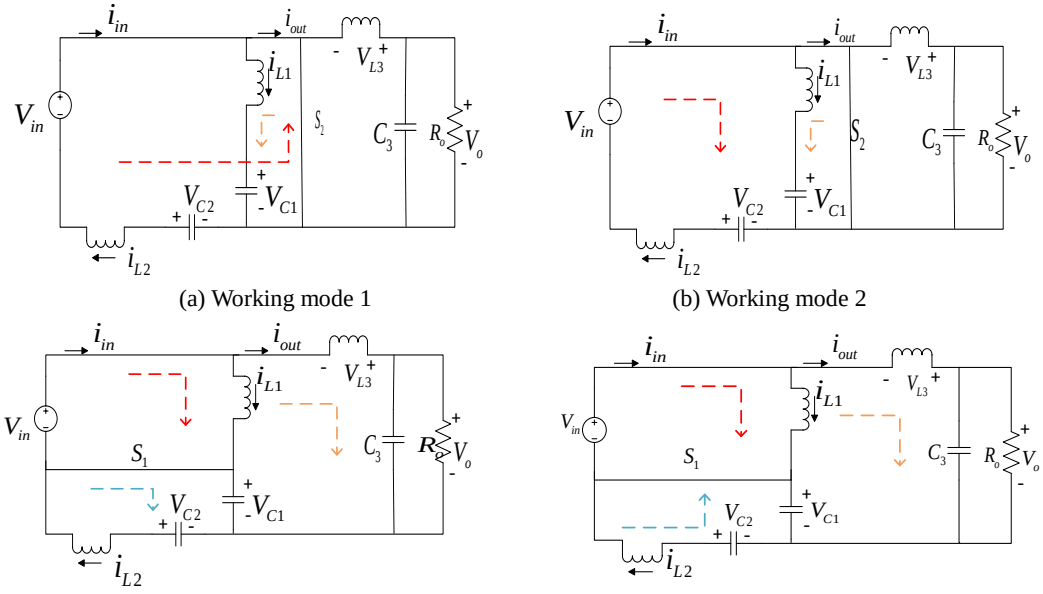


Figure 4. Four working modes in one period

(1) working mode 1: switch S_2 is on, inductors L_1 and L_2 bear reverse voltage, the current through the inductor L_1 is small, the inductor L_1 release energy, simultaneously charging the capacitor C_1; inductor L_2 release energy, also the capacitor C_2 is charged.

(2) Working mode 2: switch S_2 is on, inductors L_1 and L_2 bear reverse voltage, the current through the inductor L_1 is to decrease to zero, the current through the inductor L_2 positive increases to maximum value; in this mode, the DC power supply, inductor L_1 and a capacitor C_2 release energy, inductor L_2 and capacitor C_1 is charged.

(3) Working mode 3: switch S_1 is on, inductors L_1 and L_2 bear reverse voltage, the current through the inductor L_1 is increasing, the current through the inductor L_2 is reduced to zero; in this mode, DC power supply, inductance L_2, capacitor C_2 release energy, the inductor L_1 and capacitor C_1 is charged.

(4) Working mode 4: switching S_1 is on, inductors L_1 and L_2 bear positive voltage, inductors L_1 and L_2 energy storage end; capacitor C_1 release energy, the capacitor C_2 and the inductor L_2 is charged.

The inductor voltage and current waveform of the proposed topology is shown in Figure 5, which proves the correctness of the aforementioned analysis.

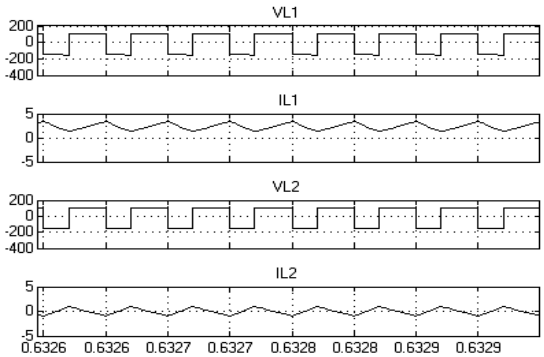


Figure 5. Inductor voltage and current waveform

3 Parameter design and circuit simulation

3.1 Parameters design

The selection of parameters in the literature [7] has been described; here no longer introduces it detailed. The selection of inductance is mainly related to the current flowing through the inductor.

Assuming that switch S_2 is on, the inductance L_1 release energy,the inductance current declines linearly.Assuming that the inductor current ripple x% is 10%, the inductance value can be calculated:

$$L_1 = \frac{v_{L1}dt}{di_{L1}},\quad di_{L1} = x\%\, I_L,\quad L_1 = L_2 = \frac{V_{C1}T_0}{2I_L x\%}.$$

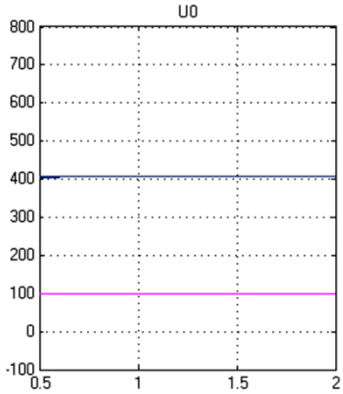
The capacitor C1 and C2 are used to absorb the high frequency current component to ensure that the output voltage is stable, assuming that the capacitor voltage ripple r% is 1%, and the capacitance value is calculated:

$$C_1 = \frac{i_{C1}dt}{dV_{C1}},\quad dV_{C1} = r\%\, V_{C1},\quad C_1 = C_2 = \frac{I_{L1}T_0}{2V_{C1}r\%}.$$

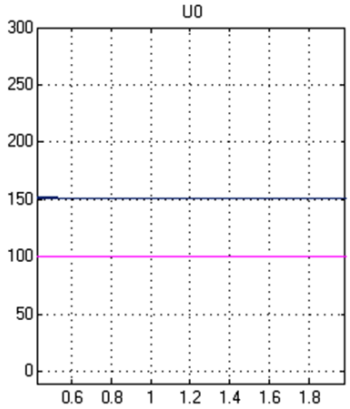
According to the literature and the principle of the circuit, the main circuit parameters are as follows: $V_{in} = 100V$, $L_1 = L_2 = 500uH$, $C_1 = C_2 = 330uF$, $L_3 = 1.5mH$, $C_3 = 22uF$,switching frequency $f_s = 20kHz$.

3.2 Simulation verification

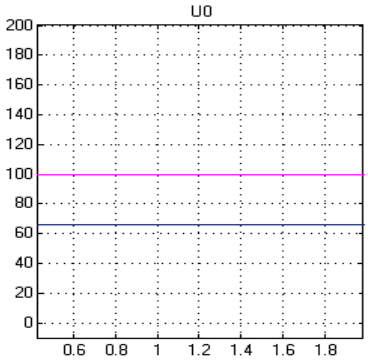
Using MATLAB/SIMULINK to simulate the new converter, under the condition of D=0.2, D=0.4, D=0.6, respectively. The simulation results verify that the topology has the wide range of buck-boost function. The simulation results are shown in figure 6.



(a) D=0.2, output voltage waveform



(b) D=0.4, output voltage waveform



(c) D=0.6, output voltage waveform

Figure 6. Output voltage waveforms of different duty cycle

4 Conclusions

The rationality of the new topology is verified by the simulation results and the theoretical deduction. Compared with other topology, the boost range of the new topology is wider; it has the advantages of simple structure, small number of devices, thereby reducing the workload of the device selection and investigation; and it has the advantages of small volume, light weight, low cost, easy to realize miniaturization.

The topology is also inadequate in some respects. The voltage stress of the capacitor C1 increases with the increase of the output voltage, and the circuit needs to be further improved when a large voltage gain is needed.

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